Measuring Charge Carrier Mobility in Graphene

Christina A. Harmon
Linfield College

Follow this and additional works at: https://digitalcommons.linfield.edu/physstud_theses

Part of the Biological and Chemical Physics Commons, and the Condensed Matter Physics Commons

Recommended Citation
https://digitalcommons.linfield.edu/physstud_theses/13

This Thesis (Open Access) is brought to you for free via open access, courtesy of DigitalCommons@Linfield. For more information, please contact digitalcommons@linfield.edu.
Measuring Charge Carrier Mobility in Graphene

Christina Harmon

A THESIS

Submitted to

The Department of Physics
LINFIELD COLLEGE
McMinnville, Oregon

In partial fulfillment
Of the requirements for the degree of
BACHELOR OF SCIENCE

May, 2015
THESIS COPYRIGHT PERMISSIONS

Please read this document carefully before signing. If you have questions about any of these permissions, please contact the DigitalCommons Coordinator.

Title of the Thesis:

Measuring Charge Carrier Mobility in Graphene

Author's Name: (Last name, first name)

Harmon, Christina

Advisor's Name

Dr. Michael Crosser

DigitalCommons@Linfield is our web-based, open access-compliant institutional repository for digital content produced by Linfield faculty, students, staff, and their collaborators. It is a permanent archive. By placing your thesis in DigitalCommons@Linfield, it will be discoverable via Google Scholar and other search engines. Materials that are located in DigitalCommons@Linfield are freely accessible to the world; however, your copyright protects against unauthorized use of the content. Although you have certain rights and privileges with your copyright, there are also responsibilities. Please review the following statements and identify that you have read them by signing below. Some departments may choose to protect the work of their students because of continuing research. In these cases, the project is still posted in the repository but content will only be accessible by individuals who are part of the Linfield community.

CHOOSE THE STATEMENT BELOW THAT DEFINES HOW YOU WANT TO SHARE YOUR THESIS. THE FIRST STATEMENT PROVIDES THE MOST ACCESS TO YOUR WORK; THE LAST STATEMENT PROVIDES THE LEAST ACCESS.

X I agree to make my thesis available to the Linfield College community and to the larger scholarly community upon its deposit in our permanent digital archive, DigitalCommons@Linfield, or its successor technology. My thesis will also be available in print at Nicholson Library and can be shared via interlibrary loan.

OR

I agree to make my thesis available only to the Linfield College community upon its deposit in our permanent digital archive, DigitalCommons@Linfield, or its successor technology. My thesis will also be available in print at Nicholson Library and can be shared via interlibrary loan.

OR

I agree to make my thesis available in print at Nicholson Library, including access for interlibrary loan.

OR

I agree to make my thesis available in print at Nicholson Library only.

Updated April 2, 2012
NOTICE OF ORIGINAL WORK AND USE OF COPYRIGHT-PROTECTED MATERIALS:

If your work includes images that are not original works by you, you must include permissions from original content provider or the images will not be included in the repository. If your work includes videos, music, data sets, or other accompanying material that is not original work by you, the same copyright stipulations apply. If your work includes interviews, you must include a statement that you have the permission from the interviewees to make their interviews public. For information about obtaining permissions and sample forms, see http://copyright.columbia.edu/copyright/permissions/.

NOTICE OF APPROVAL TO USE HUMAN SUBJECTS BY THE LINFIELD COLLEGE INSTITUTIONAL RESEARCH BOARD (IRB):

If your research includes human subjects, you must include a letter of approval from the Linfield IRB. For more information, see http://www.linfield.edu/irb/.

NOTICE OF SUBMITTED WORK AS POTENTIALLY CONSTITUTING AN EDUCATIONAL RECORD UNDER FERPA:

Under FERPA (20 U.S.C. § 1232g), this work may constitute an educational record. By signing below, you acknowledge this fact and expressly consent to the use of this work according to the terms of this agreement.

BY SIGNING THIS FORM, I ACKNOWLEDGE THAT ALL WORK CONTAINED IN THIS PAPER IS ORIGINAL WORK BY ME OR INCLUDES APPROPRIATE CITATIONS AND/OR PERMISSIONS WHEN CITING OR包括ING EXCERPTS OF WORK(S) BY OTHERS.

IF APPLICABLE, I HAVE INCLUDED AN APPROVAL LETTER FROM THE IRB TO USE HUMAN SUBJECTS.

Signature ___________ Signature redacted _______ Date 5-18-15

Printed Name ___________ Christina Harmon _______

Approved by Faculty Advisor ___________ Signature redacted _______ Date 5/18/15

Updated April 2, 2012
Thesis Acceptance
Linfield College

Thesis Title: Measuring Charge Carrier Mobility in Graphene
Submitted by: Christina Harmon
Date Submitted: May, 2015

Thesis Advisor:  
Signature redacted
Dr. Michael Crosser

Physics Department:  
Signature redacted
Dr. Jennifer Heath

Physics Department:  
Signature redacted
Dr. Joelle Murray
Abstract

This research reports measurements of electron mobility in Graphene Field Effect Transistors (GFET), gated with liquid. Mobility is a quantity describing how easily charge carriers move through a material. GFET biosensors have the greatest sensitivity when the mobility is high; therefore, increasing mobility should improve sensitivity of these and similar devices. An optimal method was established for preparing samples and taking measurements of a liquid-gate device. Sheet conductivity was measured using van der Pauw geometry and carrier density was determined from measurements of the liquid-gate capacitance. It is shown that mobility improves after the graphene surface is cleaned by an annealing process.
# Table of Contents

Abstract .......................................................................................................................... ii

I. Introduction .................................................................................................................... 1

II. Theory .......................................................................................................................... 8
   2.1 Capacitance ............................................................................................................. 8
   2.2 Mobility .................................................................................................................. 9
   2.3 Two-Probe and Four-Probe Devices .................................................................... 11
   2.4 Van Der Pauw ...................................................................................................... 12

III. Methods ..................................................................................................................... 16
   3.1 Wafer Preparation .................................................................................................. 16
   3.2 Etching Graphene ................................................................................................ 18
   3.3 Transferring Graphene ......................................................................................... 19
   3.4 Tube Furnace ........................................................................................................ 23
   3.5 Photolithography .................................................................................................. 25
   3.6 Evaporation .......................................................................................................... 32
   3.7 Lift Off ................................................................................................................... 34
   3.8 Electrical Measurements ...................................................................................... 35

IV. Results and Analysis ................................................................................................. 37

V. Conclusion .................................................................................................................. 43

VI. Acknowledgements .................................................................................................... 44

References ..................................................................................................................... 45
List of Figures and Tables

1.1 Diagram of resistance across device.................................................................2
1.2 Density of states diagram..................................................................................3
1.3 Resistance data..................................................................................................3
1.4 Varying conductivity slopes.............................................................................5
1.5 Back-gate and top-gate devices.......................................................................6
1.6 Adaptation of Cheng’s conductivity curve.....................................................7
2.1 Two-probe GFET circuit...................................................................................11
2.2 Four-probe GFET circuit..................................................................................12
2.3 Van der Pauw contacts: side versus corners................................................13
2.4 Van der Pauw geometry..................................................................................14
3.1 Cutting wafer....................................................................................................17
3.2 Breaking chips..................................................................................................18
3.3 Transfer process schematic.............................................................................19
3.4 Spin coater..........................................................................................................20
3.5 Transfer baths..................................................................................................19
3.6 Tube furnace......................................................................................................24
Table 3.1 Transfer process.....................................................................................25
3.7 Light exposure...................................................................................................26
3.8 Photolithography setup....................................................................................27
3.9 Automatic exposure control unit......................................................................28
3.10 Photolithography process...............................................................................28
3.11 Photolithography patterns...............................................................................31
Table 3.2 Photoresist exposure times....................................................................32
3.12 Evaporation chamber.....................................................................................33
3.13 Evaporated molecule paths............................................................................34
3.14 Completed device............................................................................................35
3.15 Probe station...................................................................................................36
3.16 Voltage source................................................................................................36
4.1 Size test resistivity graph……………………………………………………………………...37
4.2 Resistance data……………………………………………………………………………………38
4.3 Supplementary size resistance data……………………………………………………………39
4.4 Conductivity data………………………………………………………………………………...40
4.5 Pre/post annealing conductivity data…………………………………………………………...42
I. Introduction

The analysis and investigation of graphene is a fairly recent development. Konstantin Novoselov and Andre Geim were awarded a Nobel Prize in Physics in 2010 recognizing their pioneering investigation into the properties of graphene. Their first work was published in 2004 [1]. Graphene has numerous properties that different groups are studying and utilizing: strength, thermal conductivity, electrical conductivity, optical properties, and two-dimensionality. The applications for graphene are innumerable. Some of the ideas circulating are for use in electronics, biological engineering, filtration, strong lightweight composite materials, photo voltaics, and energy storage. This research investigates how it can be applied to a biological sensor utilizing its two-dimensionality and conductive properties. Not only can these properties be analyzed, investigation can be conducted in the improvement of these properties.

Graphite is an allotrope of carbon in which the bulk structure is composed of 2-D sheets that stack together. When there is only one layer of this carbon it is called graphene. Each layer is only one atom thick, the only height associated with it is the height of the carbon atom. Graphene is also ambipolar; this means that it has both electrons and holes that move around freely. These are referred to as charge carriers.

Graphene also exemplifies conductive properties; this is unique in the field of two-dimensional materials. Novoselov and Geim found that resistance changes as an applied voltage is changed [1]. If gate voltage, \( V_G \), was applied, inducing an electric field perpendicular to the graphene sheet, and swept across a range of voltages, it is expected that the resistance would change as the voltage changes (figure 1.1). This is because graphene is full of charge carriers.
With no gate voltage applied, graphene is close to its Dirac point (as shown in figure 1.2). This means there are no available electronic states for charge carriers to move into, thus no current flows. The total number of states per unit volume, per unit energy, is called the density of states, \( N(E) \). The further away from the Dirac point the material is pushed, the more states are available to charge carriers. Thus, it is expected that closer to the Dirac point the resistance will be greater [1]. Likewise, the further away from the Dirac point, the lower the resistance because there will be allowed states for the charge carriers to move into, thus allowing current flow. The Dirac point should ideally be around \( V_G=0V \) because that is when no voltage is being applied to cause a shift in charge carrier density. Graphene does in fact display this behavior, as shown in figure 1.3.

*Figure 1.1. Applied gate voltage to device and measuring resultant resistance.*
Figure 1.2. Density of states diagram. With more voltage applied the available states increases from 0, the Dirac point.

Figure 1.3. (a) Plot of resistance of graphene as gate voltage is swept from -0.5 V to +0.5 V. The voltage producing the highest resistance is defined as the Dirac point, and gets lower as the voltage gets further from the Dirac point. The Dirac point is close to zero. (b) Sheet conductivity versus the gate voltage. The opposite of the resistance graph is true for the conductivity graph, as it should be. The lowest conductivity is correlated with the Dirac point.
Decreased resistance can also be understood as increased conductivity, due to a greater number of free charge carriers [1]. As can be seen in equation 1.1 there is motivation to control and increase the number of charge carriers: to increase the conductivity of the graphene.

\[
\sigma = \mu n_e\epsilon
\]  

Where \(\sigma\) is the conductivity of the charge carriers in graphene, \(\mu\) is the mobility, \(n_e\) is the number of charge carriers present, and \(\epsilon=1.602\times10^{-19}\) C is a constant, the charge of an electron. Mobility describes how easily electrons move through a material. If the electrons can more easily move through the material, then any change in the environment will cause a greater change in resulting conductivity. When the voltage applied is held constant the conductivity will also remain constant. However, if something changes the voltage by acting on the surface or affecting the charges in the material, it will be detected by the resulting change in conductivity (figure 1.4). This makes graphene an ideal candidate for a biosensor. A biosensor would detect changes in location and behavior of microscopic organisms like cells and bacteria. Graphene’s sensitivity is high enough that it can detect changes in organisms of this scale [2]. Also shown in figure 1.4 is how increasing the mobility (slope of the conductivity curve, shown by equation 1.2) will increase the sensitivity.

\[
\mu = \frac{\delta \sigma}{\delta V_G} \frac{1}{\epsilon}
\]

In equation 1.2, \(C\) is the capacitance. The same amount of change in voltage on the device in figure 1.4a as on the device in figure 1.4b results in different changes in conductivity. If there is a more drastic change in conductivity for the same amount of voltage change that means the device is more sensitive. It reacts more highly to the same amount of change. This also means it is possible to detect smaller changes. In the device with lower mobility (figure 1.4a) a small
change may not appear to have any conductivity change but on the device with higher mobility (figure 1.4b) that small change would be more noticeable.

The gate voltage can be applied in two different ways: by a back-gate (figure 1.5a) that would connect to metal on the back of the substrate supporting the graphene, or a top-gate (figure 1.5b) that would connect through metal or liquid on the surface of the graphene.
Figure 1.5. (a) Back-gate graphene device with parallel plate capacitor representation. (b) Liquid top-gate graphene device with parallel plate capacitor representation. Notice the separation of charge is smaller and separated across the graphene/liquid barrier rather than the oxide.
A biological sensor would need to be able to replicate the organisms’ environment, so a liquid top-gate is a great choice. However, mobility in a liquid top-gate device is not very high as shown in figure 1.6. This puts a limit on the accuracy and size of organisms it can detect. This study explores methods to improve the mobility of liquid top-gate devices. Cheng et al found that the mobility of graphene in air was around 4,000-5,000 cm²/V*s [3]. This is higher than what they found for the mobility of graphene in solution which was around 380 cm²/V*s as shown in figure 1.6 [3]. It is thus expected that mobility in liquid will be much lower than mobility in air; but the goal is to improve the mobility in liquid.

![Figure 1.6. Adaptation of data by Cheng’s et al. [3] of gate voltage versus conductance curve taken with a two-probe measurement.](image)

---

Figure 1.6. Adaptation of data by Cheng’s et al. [3] of gate voltage versus conductance curve taken with a two-probe measurement.
II. Theory

2.1 Capacitance

Graphene can be developed into a device that mimics behavior similar to a transistor. Simply for this reason these devices are referred to as graphene field effect transistors (GFET) [4]. In a typical measurement voltage is applied to the gate on the back of the substrate while the current and resistance across the graphene are measured. There are two areas where charge carriers collect (figure 1.5a): on the graphene and on the conductive substrate in contact with the back-gate, in this case silicon. This separation of charge creates a parallel plate capacitor [5,6]:

$$C = \frac{\kappa A}{d} \quad (2.1)$$

Where $C$ is the capacitance, $\kappa$ is the dielectric constant of the material, $\varepsilon_0$ is the permittivity of space, $A$ is area, and $d$ is the distance of separation of charge. In a back-gate device $d$ is around 300 nanometers since this thickness makes graphene visible [7], the thickness of the insulating silicon oxide as seen in figure 1.5a [7]. Graphene has an intrinsic capacitance as well, called the quantum capacitance, $C_Q$ [6]. This is because in an ideal situation at the Dirac point electrons are unable to move to another state because all the places are full (figure 1.2), thus causing a separation of charge referred to as the quantum capacitance [8]. These two capacitors are in series and added as:

$$C = C_p + C_Q \quad (2.2)$$

The quantum capacitance does not have an effect in a back-gate device because it is much bigger than the parallel plate capacitor; in a liquid-gate device, however, this quantum capacitance must be taken into account because both capacitances are similar in magnitude. This is a result of a decrease in $d$. This is especially helpful because to properly mimic a biological environment, a
liquid should be used on the surface of the graphene shown in figure 1.5b. Instead of putting the
gate voltage probe on the back of the device, it is put in a salt liquid solution on the surface of the
graphene. An example of this is shown in figure 1.5b. In this device the separation of charge is
between the ions in the liquid and the charges in the graphene. The distance between them is on
the order of one nanometer rather than the 300 nanometers of the back-gate. In the liquid there is
high conductance and in the graphene there is high conductance, but to cross the separation
between the two is more difficult. This is due to the two different types of charge carriers, one is
due to ions and the other is due to electrons. With the decrease in \(d\), the parallel plate capacitance
is much higher and the quantum capacitance can be measured because it is much smaller than the
parallel plate capacitance [6].

2.2 Mobility

The amount of voltage applied will affect graphene’s electronic properties. The gate
voltage must be swept from -100V to +100V because the separation of charge is so large with
the back-gate configuration [1]. Another benefit of the liquid top-gate GFET is a lessening of
how much gate voltage is required when \(d\) is decreased. Now the voltage sweep is roughly -1 V
to +1 V, two orders of magnitude less than the back-gate GFET. The further away from zero the
gate voltage is, the higher the number of charge carriers are present [1], which will result in
higher mobility. Mobility is a measure of how freely charge carriers move through the graphene.
GFETs are more sensitive to changes in external fields when the mobility is high therefore
increasing the mobility will improve sensitivity [9]. If charge carriers can move easily without
interference it becomes quite sensitive. If the mobility is high then a small amount of voltage
change leads to a greater change in conductivity. When something comes along to interfere
either physically or by altering the electric field, that interference can more easily be detected
rather than getting lost in the noise. Disturbance of the free flowing charge carriers are indications of changes in the external fields. Detection of changes in the environment is the basis of a detector. The more sensitive the detector, the more efficient it is and the wider range of application it has.

Starting with the definition of capacitance,

\[ Q = CV \]  

(2.3)

But in this case,

\[ Q = n e \]  

(2.4)

So, the conductivity of the graphene (equation 1.1) becomes

\[ \sigma = Q \mu = CV \mu \]  

(2.5)

Substituting in equation 2.3,

\[ \sigma = CV \mu \]  

(2.6)

Solving in terms of \( \mu \),

\[ \mu = \frac{1}{CV} \]  

(2.7)

The other piece to this equation is conductivity, \( \square \). As shown, a steeper conductivity slope results in higher mobility thus increasing the GFET’s sensitivity [4]. As shown in the graph in figure 1.3a, as the gate voltage is swept the resistivity increases at the Dirac point and decreases further away. Conductivity is simply the inverse of resistivity (figure 1.3b), the degree to which electrons can move through a material. So the conductance is highest when the gate voltage is furthest from its Dirac point.

When the gate voltage is plotted versus the conductivity, mobility is the slope of the curve shown from equation 2.7. Data can be compared from measurements in liquid and air and it is shown that measurements in air are at least two orders of magnitude higher than in liquid
So measuring carrier mobility in liquid introduces some problems [10]. The purpose of this research is to investigate what those problems are and how to overcome them.

2.3 Two-Probe and Four-Probe Devices

In the literature, most reported liquid-gate measurements are conducted with a two-probe device. A schematic of a two-probe GFET is shown in figure 2.1. In a two-probe device, voltage is applied by the gate and current can be measured across the device as a function of the gate voltage [11]. From those two measurements resistance can be calculated. However, this resistance includes contact resistances. In a four-probe device (sample schematic in figure 2.2), both current and voltage are measured across the device and resistance can thus be calculated from those pieces of information [11]. Using the four-probe design gives a more accurate measurement because the voltage is measured across the graphene rather than using the applied voltage data [4, 9].

![Two-probe GFET schematic](image)

**Figure 2.1.** Two-probe GFET schematic. Current flows through the device and can be measured.
There are multiple ways to approach the four-probe design. There is still an issue of contact resistance similar to the two-probe design. Another problem that some designs have is a proximity effect: an induced electric field caused by the presence of metal leads across the graphene. This makes the mobility measurements less accurate. These problems arise from the voltage leads that lay across the graphene [11]. Putting metal so close causes an electric field closely surrounding the leads thus giving inaccurate readings for mobility. This design measures the voltage difference between the leads which leaves very little area to for the measurement to take place also decreasing the accuracy.

2.4 Van Der Pauw

An original concern with the four-probe method was how the size of the graphene would affect the measurements. Most prior experiments used graphene on the scale of less than ten micrometers but this project utilized much larger samples; between four micrometers to 200 micrometers. There are two different styles of probes that are tested: one had leads that spread
out from the sides of the device, and the other connects to the corners of the device shown in figure 2.3. Connecting the probes to the side of the device is best for smaller devices because the corners are too small for connections. Connecting at the corners is best for larger devices because the side connection introduces electric field interference from the other probes of the device and some contact interference with the other sides.

Figure 2.3. Van der Pauw designs. (a) Corner geometry; best for bigger sizes. (b) Side geometry; best for smaller sizes.

In order to address this concern and some of the issues incurred by a typical four-probe measurement like the contact resistance, the van der Pauw method was adopted. The requirements to follow the van der Pauw method are: an arbitrary shape, thin film material, small contacts located on the edge of the sample, and a homogenous material lacking in defects and holes [12]. This method is unaffected by the size of the sample and it provides more open surface
to measure voltage. This method requires measuring the voltage across the sample and the current in the perpendicular direction, then rotate the sample leads 90 degrees and measure both again [12]. From figure 2.4 that means measuring $V_{AB}$ and $I_{CD}$ then measuring $V_{CD}$ and $I_{AB}$. As before, this will result in resistance data which can be used to derive the conductivity and mobility.

Ohm’s law states $V=IR$, so for this geometry:

$$ R = \frac{V}{I} \tag{2.7} $$

As well as:

$$ R = \frac{V}{I} \tag{2.8} $$

Van der Pauw’s equation is [12]:

$$ \frac{2}{R} = \frac{1}{V} + \frac{1}{I} \tag{2.9} $$

The devices were fabricated to be symmetrical, so it is assumed

$$ R_{AB} = R_{CD} \tag{2.10} $$

$$ R_{DA} = R_{CB} \tag{2.11} $$

**Figure 2.4.** Van der Pauw device schematic. Measure $V_{AB}$ and $I_{CD}$ then $V_{CD}$ and $I_{AB}$. If the sample is a square the measurement can be assumed to be identical both ways.
Where

\[ R = R_{\text{shunt}} R_{\text{series}} \]  \hspace{1cm} (2.12)

Rearranging,

\[ \rho = \frac{R}{\rho_{\text{square}}} \]  \hspace{1cm} (2.13)

Now as shown in equation 2.13 the measured resistance can be converted into the square conductivity, \( \rho_{\text{square}} \), and plotted to find the mobility.
III. Methods

3.1 Wafer Preparation

Graphene grown by chemical vapor deposition is the best choice for making graphene field effect transistors because it can be very high quality, single layer, and it is among the easiest methods to mass produce [13]. For this research a monolayer two inch square of graphene was obtained from ACS Material [13]. This graphene is grown on a copper substrate and must be transferred to the desired substrate before it can be of use. The substrate used to house the graphene is a silicon chip with 300 nanometers of silicon oxide on the surface [7]. Graphene alone is too thin to be seen optically, but the oxide causes refraction which makes the graphene visible under an optical microscope. The wafers tend to have a purple tint to them due to the thickness of the oxide layer.

The wafer must first be coated with a medium thickness layer of photoresist covering the polished side. This acts as a protecting layer from chemicals and any debris it may come into contact with; especially during the cutting process. The layer of photoresist is painted on with a brush under red light. The whole wafer is resting polished side up on a hotplate turned off until completely painted. Then it is turned on to 60 degrees Celsius for 15 minutes taking caution to not let the photoresist burn. A wafer is about six inches in diameter, while the size used for a device is 1 cm x 1 cm. After drying the wafers can be cut with a diamond cutter. It is simplest to cut the whole wafer at once. The wafer is laid with photoresist side down on a Kimwipe. Using a ruler, marks are made every centimeter with the edge of the diamond cutter. The direct tip is avoided to delay dulling. Using the diamond cutter a grid is etched into the whole wafer before fully cutting through as shown in figure 3.1. Cuts are made very firmly and along a ruler edge.
As the cut gets closer to breaking through, it can be snapped apart by firmly placing a new or clean (rinsed with acetone, isopropyl alcohol, and deionized water then dried with nitrogen gas) slide along the break edge while a slide is placed underneath for a cliff-like edge, using a third slide pressure is applied to the chip slightly off the desired edge to be broken. This is shown in figure 3.2. While firmly applying pressure the chip will snap apart. The edge pieces cut from the wafer are not used because the oxide may not be as smooth and in good condition around the edges of the wafer. After the wafer has been cut up completely, the pieces are plasma oxide etched for four minutes to remove any particles on the surface.

**Figure 3.1.** Using a diamond cutter to cut the wafer into chips. The diamond cutter is at an angle to help preserve the tip. Each chip will be 1x1cm.
3.2 Etching Graphene

The chips are first oxygen plasma etched to remove any organic material. The chips are put into a plasma etcher for four minutes under a vacuum system. This process uses pure ionized oxygen gas. Since the ionized oxygen is so reactive it reacts with any organic material and removes it.

After the graphene is on the chip it is etched into a shape that is useful. This is done in the same manner as previously described but with a mask on the chip to protect the graphene that needs to stay on the chip. The desired pattern for this process is a square with leads outward to connect with the electrical circuit. There are four leads out, one in each corner, to comply with the van der Pauw design shown in figure 2.4 [12].
3.3 Transferring Graphene

Graphene is not strong enough to be maneuvered, nor can it be easily seen alone, so a layer of photoresist or polymethyl methacrylate (PMMA) is spun on the top of the graphene while it is still on the copper foil from the chemical vapor deposition as shown in figure 3.3a,b. Either photoresist or PMMA can be used but PMMA is the preferred method because it tends to leave behind less residue when it is removed [14]. First, a 0.75 cm x 0.75 cm square is cut from the foil. This must be done very delicately because the scissors easily wrinkle and crease the graphene which can cause defects. The foil piece is then pressed firmly between two clean slides to remove any wrinkles that may have been caused. A small (along the lines of 0.5 cm) piece of candle wax is placed on the center stand of the spin coater shown in figure 3.4, and melted with a heat gun. The graphene is immediately placed on the wax as flat as possible. Before anything else can be done the wax must be cooled. The stand can be cooled with ice carefully to help speed up the cooling of the wax.

Two drops of PMMA are placed on the copper with a pipet. After spinning the PMMA for 45 seconds at 4800 rpm, it is gently removed by the corner and dried on a hotplate for 20 minutes in air at 100 degrees Celsius. The hotplate is important because it allows the PMMA to melt a little bit and conform to the graphene; then the PMMA hardens forming a protective barrier while providing strength for maneuvering [14].

![Figure 3.3](image-url)

*Figure 3.3. Transfer schematic of graphene from copper to silicon substrate. (a) Graphene on copper. (b) PMMA spun onto graphene on copper. (c) PMMA on graphene on silicon/silicon oxide chip after etching the copper away, cleaning, and scooping onto the chip. (d) Graphene on silicon oxide chip after cleaning off the PMMA and drying.*
After drying, the graphene on the unprotected side of the copper is removed. It is then placed into a beaker with iron chloride (FeCl₃) for 24 hours shown in figure 3.5a. The iron chloride etches copper but does not react with the PMMA or damage the graphene.

After the 24 hour period has finished, the graphene is scooped out with an extra 1 cm x 1 cm silicon chip and placed in a 50 mL beaker with deionized water. An example is shown in figure 3.5b. This first bath lasts for fifteen minutes. The silicon chip can be used for the next water bath transfers if it is cleaned with acetone, isopropyl alcohol, and deionized water then dried with nitrogen gas. The next bath is just like the first but after the graphene has been scooped out with the chip and placed in the water, it is left for thirty minutes. An example of scooping out the graphene using a chip is shown in figure 3.5c. This is repeated again once more.

Figure 3.4. Spin coater used to apply photoresist and PMMA. Shown here is a piece of copper foil with graphene.
but the bath time is one hour. The baths clean the substrate better when there is more water. The point is to dilute the etchant decreasing the probability of an etchant molecule clinging to the device leaving behind clean graphene.

When the chip has finished all the water baths it is scooped out with a new 1 cm x 1 cm silicon chip that will become its permanent substrate as shown in figure 3.3c. The chip is immediately dried with nitrogen gas extremely gently from the center of the graphene out towards the edges as shown in 3.5d. This is to help flatten the graphene and remove wrinkles. It also helps the graphene adhere to the substrate by removing the residual water that creates a barrier between them. This step takes a bit longer than one might think. The graphene looks flat and adhered to the surface but as the drying is continued there is a slight darkening in color to the graphene. This is when the graphene has actually made good contact with the chip. To continue drying the chip with the graphene on it, it is now left on a hotplate in air at thirty degrees Celsius for at least three hours. An example of graphene on the silicon chip with photoresist after drying is in figure 3.5e.
Figure 3.5. (a) Iron chloride etchant (FeCl₃) with the square of PMMA, graphene and copper floating in it. (b) Deionized water bath with graphene floating to rinse the etchant off. Graphene has a layer of PMMA on it. (c) Scooping the graphene and PMMA out of the water bath on a silicon chip. (d) Drying the chip with N₂ gas very gently and patiently. (e) Silicon chip with graphene and photoresist.
The PMMA that was placed on the graphene to help transfer it must next be removed. This is done by soaking the entire chip in acetone at sixty degrees Celsius for ten minutes. It is then rinsed gently with acetone then a drop of acetone is left on the surface of the chip to protect from air dust as it is transferred to a second acetone bath at sixty degrees Celsius. It must soak here for another ten minutes. Now it is transferred to room temperature isopropyl alcohol; it is rinsed with isopropyl alcohol with a drop left on the surface again while moving the chip from one beaker to the next. This rinsing process helped prevent the resist and dust from being transferred through each bath. It also helps prevent the chip from drying in the air, which leaves water marks and dries the dirt onto the chip. The last bath is a deionized water bath for ten minutes; it is transferred using the same process as described for the first two baths just using deionized water. After all the baths have been completed it needs to be dried with nitrogen gas again using the same caution and technique as mentioned before. The final device will be the silicon chip with the layer of silicon oxide and graphene, as shown in figure 3.3d.

3.4 Tube Furnace

The final step towards transferring graphene to a silicon substrate is a bake in a tube furnace at 400 degrees Celsius for one hour. A diagram of the tube furnace is shown in figure 3.6. This final bake helps remove any excess liquid residue from between the graphene and the silicon chip as well as on the surface of the graphene; in the process a better contact between the graphene and the silicon chip is created. It also helps remove any left over PMMA residue that inevitably remained even after chemical cleaning. The tube furnace should be clean so the gas is run for 15 minutes through the gas tube in figure 3.6c. The gas consists of 95% argon and 5% hydrogen. A long hook is used to place and remove the platform that holds the chip (figure 3.6e). Before turning on the gas the seals on both ends of the tube should be tightened (figure 3.6c). As
the gas is turned on the flow meter (figure 3.6a) should be around four. This flow rate is enough to flood the tube without disrupting the sample inside. Heating up the sample should be a slow process so the tube furnace is set to the lowest heat setting (figure 3.6g). If the sample is heated too quickly, molecules under the graphene have the potential to get excited and burst through the graphene causing defects rather than wiggling out the edges and being swept away. Once the furnace gets to 400 degrees Celsius, visible by the thermometer on the front panel, figure 3.6f, bake for one hour. There is less concern of damaging the graphene during cooling so it can be quicker; turn off the oven, open the lid, and let the gas flow.

**Figure 3.6.** Tube furnace. (A) Gas flow meter (set to 4), (B) Tube furnace, (C) Gas hose and plug for tube, (D) quartz tube where the chip is located and gas flows through, (E) metal tray for the chip to rest on, (F) heat gauge, (G) temperature control dial.
After preliminary measurements are taken the device can be annealed to remove potential stray molecules on the surface of the device. Annealing is a process that heats up the material to a temperature that will loosen up the molecules enough that stray molecules will be removed from the surface completely and swept away in the flow of gases. The bonds of the graphene are strong enough to hold together and not be affected by the high temperatures. Anything else however does not so easily withstand the 400 degree Celsius heat. This annealing process is the same process as baking the chip described in section 3.4.

Table 3.1. Transfer process temperatures and times.

<table>
<thead>
<tr>
<th>Step</th>
<th>Action</th>
<th>Temp</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Spin</td>
<td></td>
<td>60 s</td>
</tr>
<tr>
<td>2</td>
<td>Hot plate</td>
<td>100°C</td>
<td>15 min</td>
</tr>
<tr>
<td>3</td>
<td>DI Bath</td>
<td></td>
<td>15 min</td>
</tr>
<tr>
<td>4</td>
<td>DI Bath</td>
<td></td>
<td>30 min</td>
</tr>
<tr>
<td>5</td>
<td>DI Bath</td>
<td></td>
<td>60 min</td>
</tr>
<tr>
<td>6</td>
<td>Dry N₂</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Hot plate</td>
<td>30°C</td>
<td>3 hours</td>
</tr>
<tr>
<td>8</td>
<td>Acetone</td>
<td></td>
<td>10 min</td>
</tr>
<tr>
<td>9</td>
<td>Rinse w/ acetone</td>
<td></td>
<td>10 min</td>
</tr>
<tr>
<td>10</td>
<td>Soak acetone</td>
<td></td>
<td>10 min</td>
</tr>
<tr>
<td>11</td>
<td>Rinse w/ IPA</td>
<td></td>
<td>12 min</td>
</tr>
<tr>
<td>12</td>
<td>Soak IPA</td>
<td></td>
<td>10 min</td>
</tr>
<tr>
<td>13</td>
<td>Rinse DI</td>
<td></td>
<td>14 min</td>
</tr>
<tr>
<td>14</td>
<td>Soak DI</td>
<td></td>
<td>10 min</td>
</tr>
<tr>
<td>15</td>
<td>Rinse DI</td>
<td></td>
<td>16 min</td>
</tr>
<tr>
<td>16</td>
<td>Dry N₂</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>Tube furnace</td>
<td>400°C</td>
<td>60 min</td>
</tr>
</tbody>
</table>

3.5 Photolithography

Photolithography is conducted to create patterns on the chip that will later be filled with metal to be circuit contacts. Photolithography is the exposure of light onto a light sensitive substrate, shown in figure 3.7, for the purpose of designing a pattern on the surface of the device.
The area of the substrate that was exposed to light will wash away when the chip is developed in photo developer, Microposit 352 Developer.

Since photoresist reacts with light, all processes involving photoresist are done in a dark room with an overhead light of roughly 655 nm (red). Photoresist is spun onto the entire surface of the chip for 60 seconds at 4800 rpm using the same technique as described earlier. It is important to spin for 60 seconds because the photoresist needs to be thin enough to work with the exposure lights; it also needs to be smooth and even across the whole chip for consistency in exposure as well as to ensure the photoresist reaches the edges of the chip. Any less time in the spin coater and the patterns will not expose correctly. The set up for photolithography is shown in figure 3.8. The pattern is transferred from the PowerPoint on the computer through the projector (figure 3.8a). The projector has a flipped lens so the image is smaller than normal rather than being projected. It is sent through the optical microscope by a 45 degree mirror that has a solid glass face extending out and down from the mirror giving the glass a triangle shape as

Figure 3.7. Patterned light exposed to the silicon substrate that has a layer of photoresist on the top.
seen from the side view (figure 3.8b). The solid glass front is important to protect the mirror from the high heat at close range created by the projector. The microscope has a shutter that is controlled by an automatic exposure control unit (figure 3.9); this lets the image through only for specified amounts of time leading to higher exposure accuracy and repeatability. When the image is allowed to go all the way through the microscope it hits the chip (figure 3.8e) with differing magnifications varying from 5x to 50x depending on which lens is positioned directly downward (figure 3.8d). The chip is brought into focus by the dial on the sides of the microscope (figure 3.8f). The amount of ambient light allowed into the microscope can be controlled by a knob on the side of the eyepiece (figure 3.8c).

Figure 3.8. Photolithography setup. (A) Projector to transfer pattern, (B) Mirror to direct light down into the microscope, (C) Knob to adjust light allowed through, (D) Lenses with varying magnifications, (E) chip location, (F) Focusing dial.
To begin the photolithography process the projector is turned on using the central power button and the PowerPoint slide is prepared in slideshow mode. The white (regular) lights in the room must be turned off and the red lights turned on. Red lights do not react with the photoresist so these are safe. The microscope has different lenses that change the color tint, it is important to make sure the lens is the green one rather than the clear one. The green also does not react with the photoresist and is safe to use thus allowing the pattern to be seen. The only other options would be red light which would not allow the positioning slide to be visible, or a white light which has a mixture of all colors including blue which would cause the whole chip to expose
instantly. The pattern used to create four probe devices is titled “Christina’s Try.ppt”. There are two versions of each pattern that needs to be exposed: a red version (R:255, G:0, B:0, with a wavelength of around 650nm) and a blue version (R:0, G:0, B:255, with a wavelength of around 475nm). When positioning the pattern, the projected slide needs to be on a red slide not blue since blue is the exposure wavelength. To view the pattern on the graphene the automatic exposure control unit must be turned on. The dial labeled ASA should be at “400”, reciprocity on “4”, exposure adj. on “1”. The mode/exposure time can be adjusted to the desired time; if a constant display is needed (for setting up the pattern in the proper location for example) then the mode/exposure time can be set to “T”. “Expose” will open the shutter and “Time off” will close it. Shown in figure 3.8c there is a knob by the eyepieces that needs to be half out when looking through at the chip; when exposing it needs to be pulled all the way out. This determines how much light can go through and when exposing it is best to block out all extra light to help focus the pattern down to the chip. When exposing, the microscope light is turned off for the same reason.

Patterns were designed in PowerPoint and exposed onto the chip. The patterns must be exposed in stages because of the sizes of the optical microscope and chip. They expand outward from four probes and gradually get larger out to pads that can be seen with the eye. This allows wires to be expanded to a size in which macroscopic connections can be made and complete the circuit. These patterns were designed for a four-probe set up, not for the van der Pauw geometry. The van der Pauw geometry is simply squares in contact with the corners of the square graphene.

There are three exposure stages. The first pattern is shown in figure 3.11a. This pattern is the second stage of wires. When setting up the pattern the red slide is used; it must be located in the right spot for the graphene as well as in focus through the microscope. The pattern must be
exposed through 5x lens on the microscope for 3.2 minutes. Then it is submerged in a developing liquid for ten seconds. When the chip is developed the areas exposed to the light are removed while the rest of the chip stays protected by the photoresist. Immediately after it must be rinsed with deionized water and dried with nitrogen gas. Then it is ready to expose the next pattern which is a simple square that acts as a pad.

Each step of the pattern that is exposed should overlap the previous to ensure connection. The patterns tend to expose slightly up and right from where the red pattern sits. This will be exposed through 10x lens for two minutes then the chip is developed for ten seconds (shown in figure 3.10a,b). The rinsing and drying process is repeated. The same square slide is used for the next exposure just through 5x instead of 10x. This is done for two minutes and developed for ten seconds. The rinsing and drying process repeats here as well.

The last pattern is the most delicate; it is the wires that make contact with the graphene and must be placed in the center of the four probe pattern previously exposed. By this point in the developing the previous four probe pattern should be quite easily seen. This last piece (figure 3.11b) is exposed through the 50x for only four seconds and developed for ten seconds. A final rinse and dry occurs here. The completed pattern should be all connected with no gaps between steps. The edges should be crisp not rough; be sure there is no over or underexposure or developing happening. If there is a mistake noticed at any stage that cannot be fixed by the further developing of the chip, simply clean the whole chip with acetone, isopropyl alcohol, and distilled water, dry with nitrogen gas, and reapply the photoresist following the previously mentioned steps. Then the chip is ready to start exposing the patterns with adjusted times or pattern locations.
Any time a new pattern is created or another variable about the setup is changed the exposure and developing times are subject to change. Before spending time exposing and developing on an important graphene device, a blank silicon chip with photoresist can be used for practice. It is best to start with shorter developing times because it can easily be developed for longer. Exposure times are adjusted to be longer if the pattern does not readily appear or is blotchy after developing; inversely, if the pattern overexposes the exposure time must be decreased. Overexposure can look like bubbled or rounded edges instead of straight edges, or overly dark coloration. It is also important to use fresh developer. If it is left out past around three hours it does not develop the chip at all.

Adjusting exposure and developer times are also critical when adding patterns to existing devices. When a device needs to be altered or needs a better connection, photolithography can be used to add leads to the existing pattern. For example, a pattern was designed on a chip but it was then realized that the pads were too small to connect the probes to; bigger pads were added to the

![Figure 3.11.](image-url)
corner squares that already existed. The device already went through the evaporation process as described below. The original pattern was done by a slightly different photolithography process. Below the layer of photoresist was a layer of lift-off resist (LOR) which helps protect the graphene from the residue photoresist tends to leave behind. This is etched away in the developing process with the photoresist that was exposed to blue light.

Table 3.2. Photoresist summary of patterns, magnification, and times.

<table>
<thead>
<tr>
<th>Step</th>
<th>Pattern</th>
<th>Magnification</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Pattern</td>
<td>3.11a</td>
<td>5 x 3.2 min</td>
</tr>
<tr>
<td>2</td>
<td>Develop</td>
<td>10 sec</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Square</td>
<td>10 x 2 min</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Develop</td>
<td>10 sec</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Square</td>
<td>5 x 2 min</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Develop</td>
<td>10 sec</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Pattern</td>
<td>3.11b</td>
<td>50 x 4 sec</td>
</tr>
<tr>
<td>8</td>
<td>Develop</td>
<td>10 sec</td>
<td></td>
</tr>
</tbody>
</table>

3.6 Evaporation

Before removing the extra photoresist a layer of chromium then a layer of gold is evaporated onto the entire chip as shown in figure 3.10c. The layer of chromium is to help the leads adhere to the surface, gold does not adhere to either silicon oxide or graphene very well. The gold is still important because it acts as the conductive wiring. One way this can be done is with a bell jar evaporator. It uses a vacuum system and heat to evaporate metals. An image of the chamber during the evaporation process is shown in figure 3.12. Another evaporation option is e-beam evaporation. This process involved targeting the metal with an electron beam under high vacuum (around 3x10^-6 Torr) which causes the atoms to change into a gaseous form and fill the chamber that has the device in it. In either process, when the evaporated molecules come into contact with the surface they solidify again thus thinly coating the device (about 200 Angstroms
thick) with the metal shown in figure 3.13. Also shown in figure 3.13 is where the molecules of metal will tend to travel. As shown there may be areas that do not get fully covered with the metal due to the angle at which the molecules fly or the device position in the chamber. The best coverage will happen when the device is directly above the chamber but if there are numerous devices and a device is not mounted directly above the metal it will have a greater angle from the metal source to the chip surface thus lower coverage. The angled area circled in red in figure 3.13 comes from the LOR reacting with the developer in newly exposed areas. The chemical will continue to react with the LOR as long as there is new surface area available.

**Figure 3.12.** Evaporation chamber. A gold bead sits on a tungsten boat at the base of the chamber. The pressure is decreased and the temperature increased until the gold evaporates upward onto the platform that has the chips mounted onto it. This platform hangs upside down so the top of the chip faces the bottom of the chamber where the gold comes from.
3.7 Lift-Off

The excess photoresist is removed by submerging the chip in 60 degree acetone, the excess metal attached to the remaining photoresist is also removed. The metal that came directly into contact with the chip where the photoresist was patterned stays on the chip; the pattern remaining with the metal now acts as the connection for the circuit shown in figure 3.10d. A completed device is shown in figure 3.14.

**Figure 3.13.** Metal being evaporated onto a substrate. The metal at the bottom is being evaporated up to the top of the chamber which includes the chip as shown. The arrows indicate the directions the metal molecules will tend to travel. The red circles indicate areas that may not get a full or even partial covering of metal thus potentially losing that circuit connection.
3.8 Electrical Measurements

To conduct data collection, the station in Ethan Minot’s lab at OSU was utilized. The four-probe station is located in a Faraday box to help protect the device from outside interference such as electric fields and charges in the air as shown in figure 3.15a. Each of the probes is lowered to make contact with their respective pad like in figure 3.15b. A few drops of 10 mM phosphate buffer with a pH of 7.1 are added to the surface of the graphene. This is the liquid top-gate. The four probes are tapered tungsten wires with pyralene c coating. The pyralene coating acts as an insulator so there is less noise caused by the probes. These are each lowered down onto the gold pads so they make gentle contact shown in figure 3.15b. Another probe is lowered into the liquid without making contact with the graphene or metal. Then the gate voltage is swept from -0.5 V to +0.5 V and back again with a power supply (shown in figure 3.16). The purpose of sweeping back again is to show reproducibility. A preamplifier was used to measure the current going

Figure 3.14. Completed device after excess metal has been removed. This device has a van der Pauw geometry and was used to collect the data. The graphene in the center has been etched. The inner squares were added using a masked photolithography. The outer squares were added later using the first process that was explained above. These squares were added to increase the area the probes would attach to.
through the device. This was a small current that was kept constant at 200mA. If the current is too high it was start to change the graphene. When it is low the graphene acts metallic and conductive. If it is too small then it is not sensitive enough. Also a low pass filter was used set at 12dB and with a frequency of 10Hz.A LabVIEW program was used to automate data collection. Then after the gate voltage has finished sweeping the result is a curve of $V_G$ versus resistance. All the data needed for the conductivity can be collected from this process.

(a)       (b)

Figure 3.15. (a) The entire four-probe set up as well as the top-gate probe. The set-up is in a box to prevent other electrical interference and under a microscope to assist with placing the probes gently. (b) Closer view of the four-probe set up. The three of the four probes are set down on the device

Figure 3.16. Power supply. The power supply goes to the probe in the liquid itself thus acting as the gate voltage.
IV. Results and Analysis

To test the credibility of the van der Pauw method sample devices made of metal were measured. Rather than connecting gold leads to graphene, the center of the device had a layer of gold with thickness 50 nm instead. There are two different styles of probes that are tested: one had leads that spread out from the sides of the device (blue), and the other connects to the corners of the device (red) (see figure 2.3). The accepted resistivity for gold is $2.24 \times 10^{-8} \Omega \text{m}$. The measured resistivity of varying sizes is shown in figure 4.1. The resistivity is generally within the same range although higher than the accepted value; this is expected due to the evaporation process. Impurities can be implanted into the device causing a higher resistivity. The breaking point is shown in figure 4.1; the biggest area measured that works for the side connection is 25x25 $\mu$m, the smallest area measured that works for the corner connection is 32x32 $\mu$m.

![Figure 4.1](image.png)

Figure 4.1. All resistivity values are $x10^{-8} \Omega \text{m}$. There are two different styles of probes that are tested: one had leads that spread out from the sides of the device (blue), and the other connects to the corners of the device (red). The biggest area measured that works for the side connection is 25x25 $\mu$m, the smallest area measured that works for the corner connection is 32x32 $\mu$m.
Data was collected of the sweeping gate voltage and the corresponding resistance as shown in figure 4.2. These results follow the expected trends from Novoselov’s et al. research [1], a peak in resistance at the Dirac point (located close to 0V). As the gate voltage gets closer to the Dirac point the resistance increases dramatically. Further away from the Dirac point, typically further from zero, the resistance is much smaller.

Numerous devices were created and measured with this process. Figure 4.3 shows the resistance of two more devices that are different sizes. Figure 4.3a shows data from a device

![Graph showing resistance vs. gate voltage](image)

**Figure 4.2.** Original data collection from this project that follows the expected reaction of graphene in a liquid top-gate device as the gate voltage is swept from -0.5V to +0.4V. The highest resistance lies close to zero, at the Dirac point, and gets lower as the voltage gets further away.
19x19 µm and figure 4.3b shows data from a device 200x200 µm. The device shown in figure 4.2 is 50x50 µm. Despite a large range of device sizing, the resistance is very similar and follows the expected trends. There is not much fluctuation between devices even with the size difference. The fluctuation that does appear results from defects in the graphene itself, rather than the size of the graphene.

Since conductivity is the inverse of resistivity it can be seen from figure 4.4 that conductivity is lowest at the Dirac point and it increases further away from the Dirac point. There is some noticeable hysteresis present on the negative voltage side of the graph. This means that the charge carriers behaved differently when the voltage was being swept from 0V towards -V than it did when sweeping from -V to 0V, resulting in differing conductivities at the same voltage. This is likely due to some electro chemistry happening in the liquid. In order to allow the flow of electrons between the liquid and the graphene there needs to be a redox reaction, but

![Graph showing conductivity vs voltage](image)

**Figure 4.3.** Supplementary device resistance data. This shows that the van der Pauw method is not affected by the size of the graphene. (a) Resistance of a small device, 19x19 µm. (b) Resistance of a large device, 200x200 µm.
this takes some time. Each change of direction when sweeping the voltage will incur a delay because of this reaction. This means the conductivity stays the same for a short time while the voltage is changing. Between the two sides of the graph (the positive voltage and negative voltage) there is not symmetry. With better devices this should improve. One more thing to note is the rounded vertex. Since this point is indicative of the Dirac point where no charges should be moving, the vertex should be a sharp point. Since the vertex is rounded this indicated it is not an absolutely ideal situation.

![Graph of gate voltage versus sheet conductivity of graphene](image)

**Figure 4.4.** Plot of the gate voltage versus the sheet conductivity of graphene. Original data collection from this project that follows the expected reaction of graphene in a liquid top gate device as the gate voltage is swept from -0.5V to +0.4V. The lowest conductivity lies close to zero, at the Dirac point, and gets higher as the voltage gets further away.
The mobility may be easily extrapolated from this graph. From equation 2.7, mobility may be calculated by using the slope of conductivity with respect to the gate voltage, and the capacitance. The derivative of conductivity can be extracted from figure 4.4, it is 0.0028 S/V*m. From a separate project also conducted with these devices, the capacitance was measured. It was found to be 5 µF/cm² [15]. So from equation 2.7 the mobility has been calculated to be 560 cm²/V*ms. This is slightly higher than other liquid top gated measurements but within the same order of magnitude [10]. After the annealing process mobility showed improvement but still remained within the same order of magnitude shown in figure 4.5. Figure 4.6 shows the original slope laid over both the pre-annealed and post-annealed curves. The new slope of the data was 0.0036 S/V*m; thus the new mobility of the device was 720 cm²/V*ms. The data when compared to pre-annealing has a steeper and sharper vertex, as well as a shift in Dirac point as shown in figure 4.5. The shift in the graph results from a change in the electric field. A change in the electric field can result from numerous things. The most pertinent reason is the removal of excess surface charges. The graphene device had residue from the polymers put on the surface as well as molecules from the air causing interference. Through the annealing process these excess molecules and charges were removed. This means the electric field will also be changed. So the Dirac point shifts from where it laid. The hysteresis was also greatly lessened by the annealing process indicating that the molecules that caused the interference were removed.

As shown by the improvement in mobility as compared to other previous work [5,10] the van der Pauw method shows promise of being a better method of measurement. However it was still orders of magnitude lower than back gate mobility measurements [10].
Figure 4.5. Plot of the gate voltage versus the sheet conductivity of graphene. Comparing pre-annealing data (purple) and post-annealing data (green). The curve has a steeper slope that comes to a more pointed minimum. There is also the shift to the right due to the change in electric field resulting from the change in excess charges present.
V. Conclusion

By designing a GFET that utilized the van der Pauw method, the mobility of liquid-top-gate graphene was measured to be 560 cm²/V*s and improved by annealing to be 720 cm²/V*s. This shows improvement from other methods utilizing liquid-top-gate GFETs [3] but still has improvement to be made to be within the range of back gated devices. This means more research needs to go into why the liquid causes such a decrease in the flow of electrons. However, it is also shows that the van der Pauw method is a better method to utilize than the two-probe method previously applied. Through annealing the hysteresis was improved, the vertex was sharpened, and the slope was increased. Through these improvements the sensitivity of the device was also increased.

Also worth noting is this was the first four-probe configuration conducted in liquid top-gate devices. The measurements have been improved from the two-probe method by the van der Pauw method while avoiding some potentially problematic issues incurred by the four-probe design such as size and contact interference. Upon further investigation it was discovered that placement of the reference probe with respect to the graphene will affect the data. It is also necessary to do a complete van der Pauw by rotating the probes in light of the probe placement dependence rather than assuming equation 2.10. This is also to help check device connection quality.
VI. Acknowledgements

I would like to take some time to thank my husband, Bryan for all of his support, confidence, excitement, and love. Through years of research he always showed an interest in what I was doing as well voicing absolute confidence in my abilities, even if I lost faith. I would also like to thank my parents for their encouragement and love. Growing up they taught me to experiment and fed my desire to learn. Every question I asked was answered with another question that sent me on journey to understanding. There was never any question in their mind whether or not I would succeed, it was simply WHEN not IF. All through my physics career my Grandpa Larry’s encouragement and excitement has always kept me going. He too shares my passion for science and the miraculous world around us. He always encourages me to keep faith in the Greatest Scientist of all. Lastly, I would like to thank Dr. Michael Crosser. Three years ago he took on an inexperienced freshman to be on his summer research team. He saw the potential and fed it wholeheartedly. He gave me the tools I needed to make myself confident, passionate, and successful.

A special thanks to the Minot group at Oregon State University for their assistance, resources, and experience. Also thanks to the Linfield College Faculty/Student Collaborative Research Grant for the funding to pursue this project through the years.
References


