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## Searching to Distinguish Defects and the Presence of Negative Capacitance

Thaddeus Cox  
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# Searching to Distinguish Defects and the Presence of Negative Capacitance

Thaddeus J. Cox

A Thesis  
Presented to the Department of Physics  
Linfield College  
McMinnville, Oregon

In partial fulfillment of the requirements  
for the Degree of  
Bachelor of Science

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Searching to Distinguish Defects and the Presence of Negative Capacitance

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# Thesis Acceptance

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# Abstract

In the search for solar cells with lower manufacturing costs, thin film technology was developed. These thin films are only micrometers thick and are grown at relatively low temperatures, resulting in films with imperfections known as defects. Defects can cause thin film solar cells to have lower efficiencies than their single crystalline counterparts. In order to create more efficient thin film solar cells the physical mechanisms behind defects need to be investigated by sensitive techniques. Capacitance measurements of solar cells detect minute changes in charge in the material. For that reason, capacitance is used to electrically characterize the solar cell. Standard interpretations of capacitance rely on assumptions, which, if wrong, can skew the results. In some solar cells where a back contact barrier is suspected, measurements at high forward bias can be used. However at high forward bias there is an injection of minority carriers that can have an effect on the results, such as causing a negative capacitance response. We have seen that apparent signatures of a back contact barrier in  $\text{Cu}(\text{In}_x\text{Ga}_{x-1})\text{Se}_2$  might actually be the first signs of a negative contribution to capacitance. This paper will discuss the observation of negative capacitance, the possible implications of such a measurement, and its relationship to other electronic characteristics of the device.

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# 1. Introduction

## 1.1 Potential of Solar Energy and Thin Film Solar Cells

As more and more countries become industrialized, their contribution to the world's energy consumption will increase. With the increasing use of electrical energy it is important to develop electricity sources that also preserve the environment. Solar energy is one such green source.

Traditionally solar cells have been monocrystalline silicon. Monocrystalline solar cells have efficiencies around 25% [1]. This means that 25% of the optical energy from the sun that hits the solar cell is converted into electrical energy. Silicon solar cells use a lot of material and are grown under high temperatures above 1400 °C [2]. It is important to develop solar cell technology with lower production costs with the same efficiencies. With their low amount of input materials and relatively low temperature, around 550 °C growing conditions, thin film solar cells are a solution to this problem [3].

Thin films are typically not monocrystalline. The films discussed here are polycrystalline, with crystallites around two micrometers in diameter. These films are then not a perfect crystal like monocrystalline silicon. Developed thin film technologies have efficiencies around 20% [4], however there is a theoretical projection that single p-n junction devices have a thermodynamic limit allowing for a maximum efficiency of 30% [5]. The lower efficiency of thin films comes from the relatively low temperature growing conditions. When grown at these lower temperatures defects are more common. These defects could be atoms in the wrong place of the structure, atoms missing in the structure, or even bonds forming irregularly. These defects can trap charge, which would lead to a decrease in efficiency. It is important to investigate the response of these traps in order to better understand the transport of charge carriers throughout the material.

The thin film material analyzed in this work is  $\text{Cu}(\text{In}_x\text{Ga}_{1-x})\text{Se}_2$ , or CIGS for short. CIGS is a polycrystalline material that is known to have defects within the bulk material and likely also has a back contact barrier [6]. A back contact barrier is an extra energy barrier that the charge carriers need to cross near the back of the cell. Capacitance measurements detect minute changes in charge. By using capacitance measurements the response of a defect within the bulk material and a back contact barrier can be analyzed. However it is difficult to distinguish if the response is coming from a defect within the bulk material or a back contact barrier.

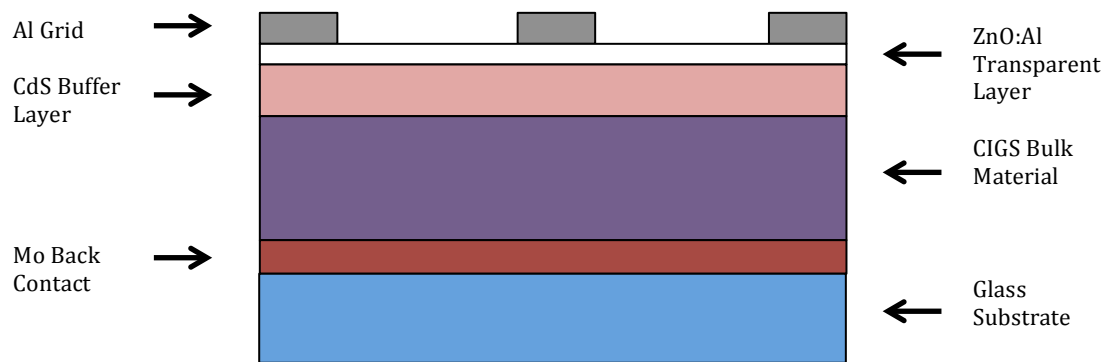
This paper is a detective story about the search to interpret the capacitance response of CIGS, in order to better understand the physics behind the defects within the cell and contribute to the increase in efficiencies of CIGS cells.

## 2. Theory

### 2.1 CIGS and the n-p Junction

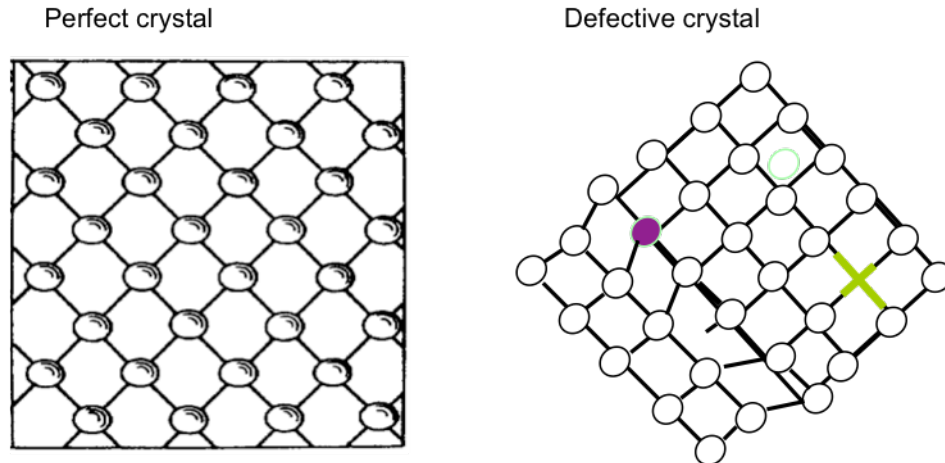
#### 2.1.1 CIGS Sample

The structure of the CIGS solar cells consisted of an aluminum contact grid, a transparent conducting contact layer of ZnO:Al, a CdS n-type layer, a CIGS p-type bulk layer, and a Mo back contact, all of which are layered onto a glass substrate. A schematic of our CIGS samples is shown in Figure 1.



*Figure 1.* Schematic for layers of the CIGS samples used.

CIGS is a polycrystalline material, meaning it does not have a perfect single crystalline structure. CIGS is known to have defects that trap charge and lower the efficiency of the cell. Possible defects within the bulk material could be atoms missing in the crystalline structure, atoms in the wrong place of the crystalline structure, or bond lengths forming irregularly. Another possible defect is a potential barrier at the back contact. The back contact barrier is an additional potential barrier that carriers will need to diffuse over in order to leave the sample to an outside circuit. The defects within the bulk material can trap charge carriers leading to a decrease in efficiency. Similarly a back contact barrier can decrease the amount of carriers that leave the sample, causing a decrease in efficiency. A schematic of monocrystalline and polycrystalline solar cells is shown in Figure 2.



*Figure 2.* Comparison of perfect (monocrystalline) material and defective (polycrystalline) material demonstrating the differences in the crystal structure. Courtesy of Dr. Jennifer Heath.

Understanding the origin of electronic responses is pivotal in the pursuit of higher efficiency CIGS solar cells. This improvement all starts with understanding the basics behind an n-p junction.

### 2.1.2 n-p Junction

An n-p junction is formed when two layers of a semiconductor material are connected. For our case the n-type semiconductor doped with electrons, is atop of the p-type semiconductor doped with holes. Holes are the absence of an electron.

In order to better describe doped semiconductors, the process of doping silicon will be described. Silicon has four valence electrons, looking to the right of silicon on a periodic table one can find phosphorous. Phosphorous is a donor dopant. This is because it has an extra electron within its valence band, so if phosphorous atoms are inserted into the silicon during crystal growth extra electrons will be in the structure. This would create an n-type semiconductor. On the other hand, aluminum has one fewer electron within its valence shell. If aluminum is injected into silicon during crystal growth, extra holes will be within the material. This would result in a p-type semiconductor material.

In contrast, the CIGS p-type doping occurs intrinsically, most likely due to the copper vacancies. No extrinsic doping was used in the formation of the samples used.

When n-type and p-type semiconductors are alone they have a neutral charge, however when they are connected a potential difference forms. A schematic of the formation of an n-p junction is shown in Figure 3.

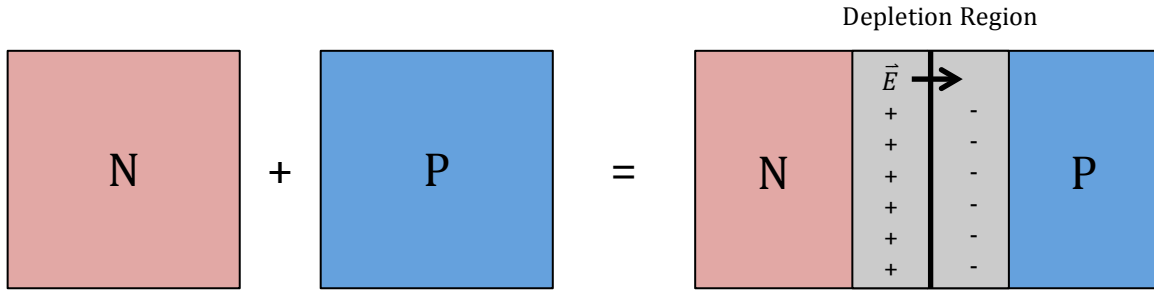


Figure 3. Schematic of the formation of an n-p junction by connecting a layer on n-type semiconductor to a layer of p-type semiconductor, causing a depletion region to form.

When n-type and p-type semiconductor materials are connected to form an n-p junction charges are exchanged. The extra holes from the p-type drift to the n-type and the extra electrons from the n-type flow to the p-type. This exchange of charge forms a region of potential difference, known as the depletion region. The depletion region is shown as the grey, labeled region in Figure 3. The potential difference causes an electric field within the depletion region, also shown in Figure 3. When a free charge enters the depletion region it will be swept out by this electric field. Free describes the ability of a charge to move throughout the material without restraint, due to its excited energy level. A band diagram of an n-p junction is shown in Figure 4.

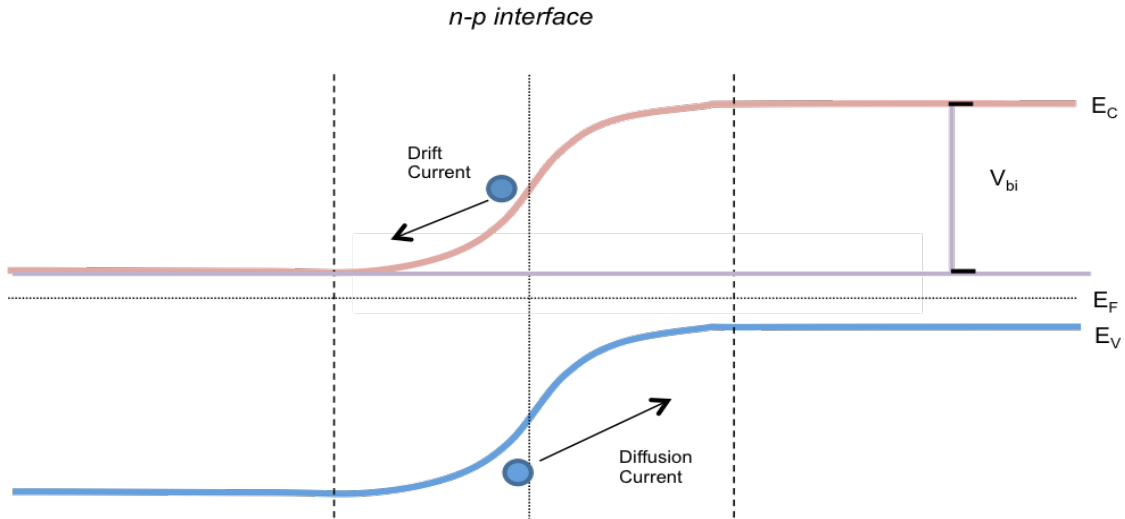


Figure 4. Band Diagram for n-p junction including electrons acting under drift and diffusion current. The  $V_{bi}$  is the built in potential difference caused by the depletion region.

Drift current describes the movement of free electrons, due to an electric field, down the potential difference of the depletion region. Diffusion current describes the movement of ground state electrons thermally diffusing up the potential difference of the depletion region to a region of higher electron density.



For our CIGS solar cell light will enter through the ZnO:Al conducting layer exciting electrons which then flow towards the n-type due to drift current. The electrons flowing from drift current can be described as a hole moving in the opposite direction. This is because a hole is the absence of an electron, so if an electron is moving one direction, a hole will move in the opposite direction.

Defects can be investigated by considering the movement of charge within a sample. Charge motion being detected by looking at the capacitance response of the sample, more specifically the differential capacitance response.

### 2.1.3 Capacitance of CIGS

Differential capacitance is mathematically represented as:

$$C = \frac{dQ}{dV} \quad (1)$$

where  $dQ$  is the change in charge and  $dV$  is the change in voltage.

When measuring differential capacitance, trends can be predicted. These predictions are based on model assumptions of an n-p junction with added DC bias. Adding a DC bias to the samples will cause a change in their band bending. The effects of DC bias on the band structures are shown in Figure 5.

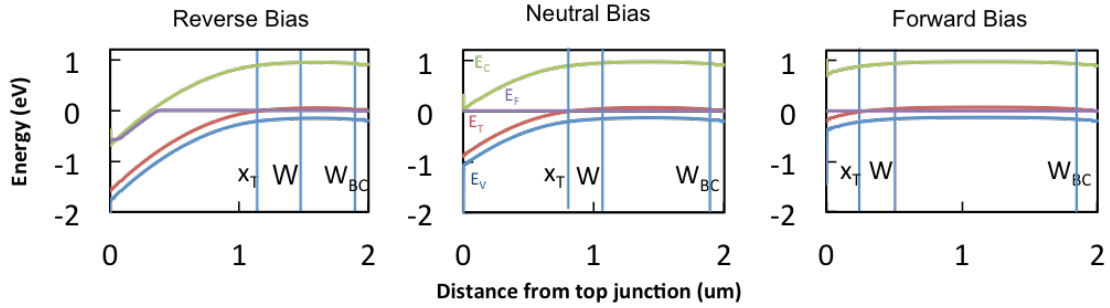


Figure 5. Band diagrams with respective applied DC bias demonstrating the band bending that occurs.

In the reverse and neutral bias regime, when differential capacitance is being measured, the capacitance can be calculated to an equation that is similar to that of a parallel plate capacitance:

$$C \approx \frac{\epsilon A}{W} \quad (2)$$

where  $\epsilon$  is the dielectric constant of the material,  $A$  is the surface area of the parallel plates, and  $W$  is the distance between the plates (depletion width of the sample).

The component of capacitance that is due to the depletion width will be referred to as depletion capacitance.

Looking at the diagrams in Figure 5, as negative bias is put on the sample the depletion capacitance will decrease. As the bias applied increases the capacitance will increase. However depletion capacitance is not the only capacitance being measured in the forward bias range. Diffusion capacitance is also being measured.

Note that as positive bias is applied, the bands are flattened. Flattening the bands causes the diffusion current to exponentially increase. In high forward bias the DC current is approximately the diffusion current. This is shown by the current equation for a diode:

$$I = I_0(e^{\frac{qV_D}{nkT}} - 1) \quad (3)$$

where  $I$  is the current,  $I_0$  is the current while in absence of light,  $V$  is the applied voltage,  $q$  is the charge of an electron,  $n$  is the ideality factor,  $k$  is Boltzmann's constant, and  $T$  is temperature.

Diffusion capacitance is capacitance that results from the injection of minority carriers. The diffusion capacitance is proportional to the injected or diffusion current, which means that it is expected to increase exponentially with an increase in forward bias being applied, based on (3).

When the junction is put into reverse bias the capacitance measurement is dominated by depletion capacitance and should decrease. When the junction is put into forward bias the capacitance measurement is a combination of depletion and diffusion capacitance. Since depletion and diffusion capacitance are both expected to increase in forward bias, the total capacitance should increase. However it has been observed that in high forward bias the capacitance measurement can decrease and even become negative.

## 2.2 Back Contact Barrier Response

The presence of a back contact barrier can be analyzed by extracting capacitance-voltage data from admittance spectroscopy. Capacitance-voltage data is the capacitance as a function of DC bias, at a constant frequency. A typical capacitance-voltage graph for our devices is shown in Figure 6.

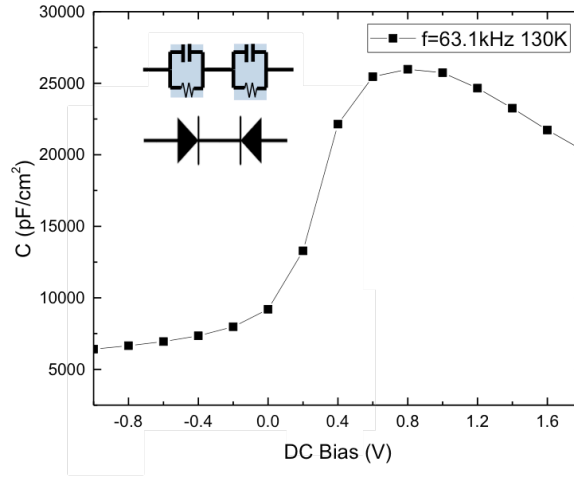


Figure 6. Capacitance voltage data showing a rollover affect that is contributed to a back contact barrier response. Inset: diagram of a double diode model.

Looking at Figure 6 and the capacitance predictions of section 2.1.1, the capacitance increases as the bias increases from negative to around the built in potential, 0.8V. Ideally the capacitance would continue to increase as the bias increases past the built in potential. However this does not occur. Instead there is a rollover effect where the capacitance starts to decrease. This has often been attributed to the presence of a back contact barrier. In reverse bias the depletion capacitance is a smaller value and dominates the measurement. At high forward bias the depletion width is approximately zero, leading to an extremely large capacitance that then takes over the measurement.

The back contact barrier response, shown as a rollover in the capacitance-voltage data, can be modeled as two diodes in series [5]. Applying bias to this model, as the first diode is put into forward bias current is allowed to flow. If the applied bias is large enough the second diode will be put into reverse bias, which would limit the current flow out of the circuit, causing a decrease in capacitance.

## 2.3 Negative Capacitance

### 2.3.1 Expected Measured Circuit

The measurements taken and analyzed within this paper are AC measurements. The AC bias,  $V$ , and the charge,  $Q$ , are changing with time, seen in (1). Manipulating (1):

$$\frac{dV}{dt}C = \frac{dQ}{dt} = I \quad (4)$$

where  $\frac{dV}{dt}$  is the change in voltage with respect to time,  $C$  is the capacitance,  $\frac{dQ}{dt}$  is the change in charge with respect to time, and  $I$  is the current.

Experimentally using (4), a small AC signal is applied, giving a known  $(\frac{dV}{dt})$  and the current  $(\frac{dQ}{dt})$  is measured. The capacitance is then calculated from the known changing voltage and the measured current. This method is expected to measure a simple circuit. A circuit diagram of the expected measurement is shown in Figure 7.

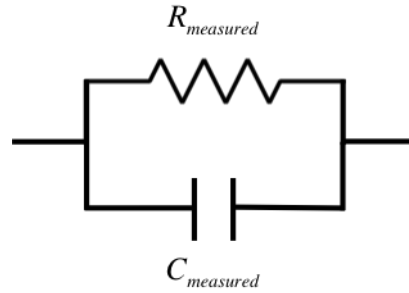


Figure 7. Circuit diagram of the expected circuit being measured.

In the simplest model of the sample,  $C_{measured}$  corresponds to the depletion capacitance from the separation of charge within the depletion region and the resistance,  $R_{measured}$ , is current leakage through the depletion region.

Within any model circuit consisting solely of resistors and capacitors, negative capacitance cannot be observed. In the AC measurement, the capacitance component of current is  $90^\circ$  out of phase from the resistance component of current. The phase diagram for the current components of resistance and of capacitance is shown in Figure 8.

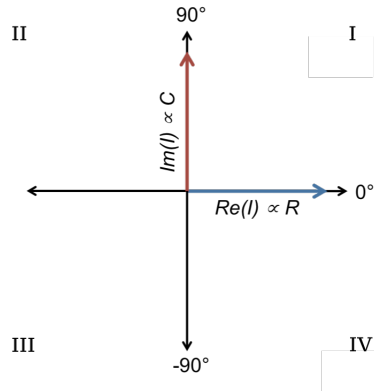


Figure 8. Current phasor diagram of the ideal circuit shown in Figure 7, to demonstrate the impossibility of measuring a negative capacitance.

By looking at the phasors in Figure 8, it is easily seen that any combination of the current components will be in the first quadrant. Since it lies within the first quadrant it will always be a positive value.

It is expected that the current measured is a positive value. The AC voltage applied is a positive value. Using a positive valued current and a positive valued voltage in (3), the resulting capacitance will always be a positive value.

However negative capacitance was measured. This means that the actual circuit cannot be modeled in the typical way. However, there is a model that describes a circuit in which negative capacitance can be observed.

### 2.3.2 Negative Capacitance Circuit Model

In the AC regime, there is a possibility that the measured value of capacitance will be negative. This is especially true in high forward bias. The model that predicts negative capacitance will be experimentally tested [7]. The circuit model from [7] is shown in Figure 9.

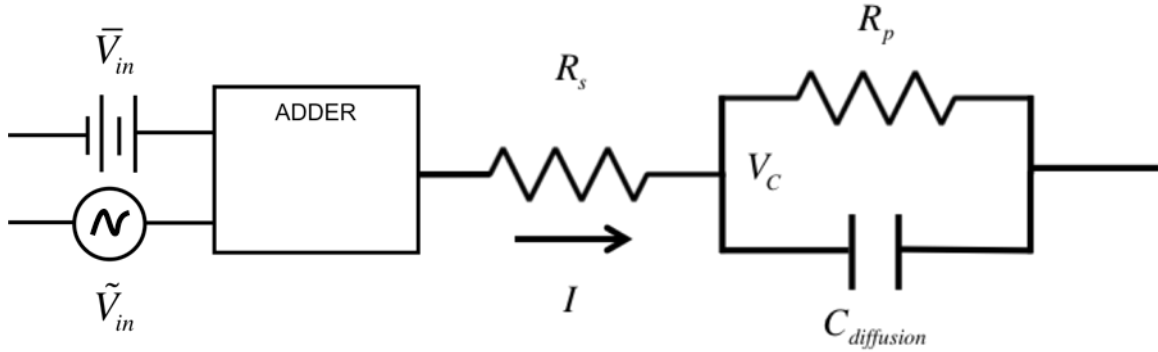


Figure 9. Circuit model including DC input voltage ( $\bar{V}_{in}$ ), AC input voltage ( $\tilde{V}_{in}$ ), series resistance ( $R_s$ ), parallel resistance ( $R_p$ ), diffusion capacitance due to the injection of minority carriers ( $C_{diffusion}$ ), voltage across the capacitor ( $V_c$ ), and the direction of current ( $I$ ).

Using circuit analysis, the input voltage for the circuit can be represented mathematically:

$$V_{in} = \bar{V}_{in} + \tilde{V}_{in}e^{i\omega t} \quad (5)$$

where  $\bar{V}_{in}$  represents the DC component of input voltage, and  $\tilde{V}_{in}$  is the AC component of input voltage, which oscillates at a frequency  $\omega$ .

In the model, the series resistance is heavily dependent on the applied voltage. This would give the series resistance AC and DC components:

$$R_s = \bar{R}_s + \tilde{R}_s e^{i\omega t} \quad (6)$$

where  $\bar{R}_s$  represents the DC component of series resistance, and  $\tilde{R}_s$  is the AC component of series resistance.

If there is a series resistance that is heavily dependent on voltage, negative capacitance is predicted. In forward bias, as the applied DC voltage increases, the series resistance will exponentially decrease. This is the same as saying that in the DC regime, the series resistance is inversely proportional to the DC current. The proportionality between series resistance and current is represented by [7]:

$$\frac{1}{R_s} = g_0 + \frac{I}{V_s} \quad (7)$$

where  $g_0$  is  $\frac{1}{R_0}$  (the inverse of the initial series resistance),  $I$  is the junction current, and  $V_s$  is a proportionality constant with the units of voltage.

For the samples used the initial series resistance is negligible. This assumption means that  $g_0$  is negligible and can be removed from (7).

The following expression describes the input voltage using circuit analysis [7]:

$$V_{in} = V_c + \frac{I_{in} V_s}{I} \quad (8)$$

Using (5), (6), and (8) the AC and DC components of the series resistance can be analyzed:

$$\tilde{V}_{in} - \tilde{V}_c = -\tilde{R}_s \bar{I} + \bar{R}_s \tilde{I} \quad (9)$$

where the first term is the AC response of the series resistance ( $\tilde{R}_s$ ) multiplied by the DC current ( $\bar{I}$ ) and the second term is the DC response of the series resistance ( $\bar{R}_s$ ) multiplied by the AC current ( $\tilde{I}$ ).

The DC series resistance term is the expected term for series resistance; the AC series resistance term is the term that arises from the heavy voltage dependence. As the applied DC voltage increases, the DC current increases due to the injection of minority carriers. By injecting charge carriers the conductance of the sample will increase, simply because there are more charges flowing through the sample. An increase in conductance is a decrease in resistance. The model predicts that if the DC current increases significantly enough the first term of (9),  $-\tilde{R}_s \bar{I}$  will dominate the measurement and result in a phase shift.

The current component from capacitance will shift phase  $180^\circ$  from its expected position. This would mean that the capacitance component of current is now  $-90^\circ$

out of phase from the resistance component of current. Figure 10 shows the current phasors for this situation.

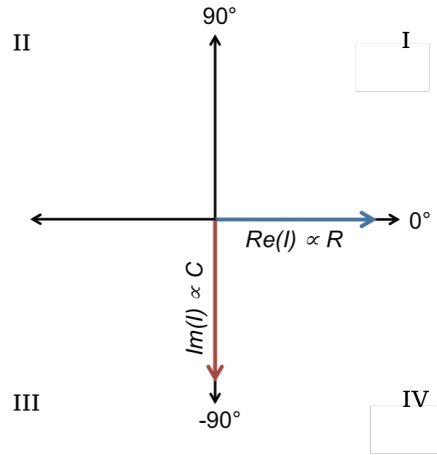


Figure 10. Current phasor diagram of resistance and capacitance to demonstrate the measuring of negative capacitance.

In Figure 10, any combination of the current components would result in a value within the fourth quadrant. A current value in the fourth quadrant will always be a negative value. This would cause the calculated capacitance to be a negative number, therefore allowing negative capacitance to be measured.

## 2.4 Admittance Spectroscopy: Capacitance-frequency

Admittance spectroscopy is the technique of applying a small AC voltage, sweeping the frequency of the AC voltage from 10Hz to 100kHz, measuring the current, and calculating the admittance. The admittance can be broken up into two components, real and imaginary. The real and imaginary admittance are represented by:

$$Y' = \frac{1}{R} \quad (10)$$

$$Y'' = \omega C \quad (11)$$

where  $Y'$  is the real admittance and  $Y''$  is the imaginary admittance.

Imaginary admittance is then used to determine capacitance values. By looking at capacitance as a function of frequency, the energy level of a trap state within the band gap of a sample can be determined. Traps are places within the sample that can decrease charge flow by trapping charge carriers. Traps could be free holes that recombine with excited electrons trying to flow out of the cell. The trapping of charge carriers will limit the movement of charge, meaning that the capacitance will change when charge carriers are free compared to being trapped. Figure 11 shows a schematic of charge carriers interacting with trap states.

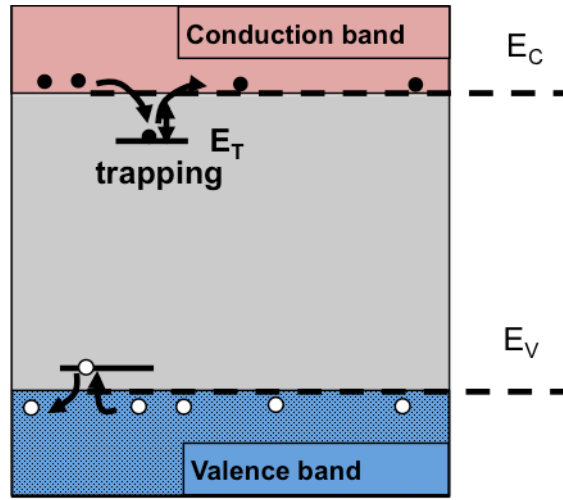


Figure 11. Diagram of conduction and valence bands with electrons and holes getting trapped and released by a defect trap state. Courtesy of Dr. Jennifer Heath.

The time it takes for charge carriers to move in and out of the traps is proportional to the energy level of the traps. The proportionality is represented by:

$$t \propto e^{\frac{E_T}{kT}} \quad (12)$$

This time corresponds to a transition frequency. At frequencies about the transition frequency the charge carriers will no longer have enough time to follow the AC voltage out of the traps, meaning they are stuck in the trap state. This will result in a capacitance response seen in Figure 12.

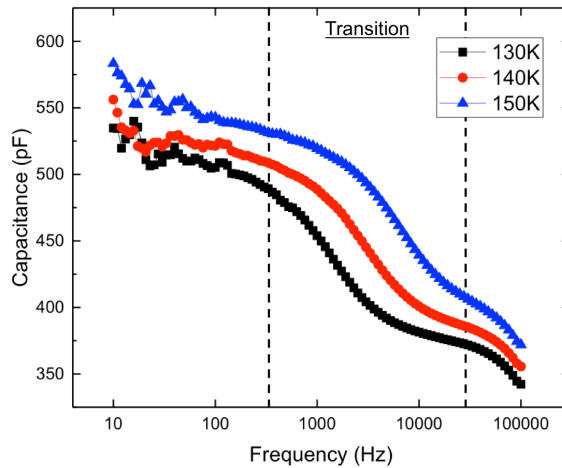


Figure 12. Typical admittance spectroscopy data representing the capacitance response for frequencies below, at, and above the transition frequency at different temperatures.



Looking at Figure 12, one can see that there is a temperature dependence of the transition frequency. Using this aspect, admittance spectroscopy was performed at multiple temperatures. The transition step from high to low capacitance can be analyzed by [8]:

$$e_n = \gamma \sigma_{na} T^2 e^{-\frac{E_{na}}{kT}} \quad (13)$$

where  $e_n$  is the electron emission from a trap,  $\gamma$  is the thermal prefactor,  $\sigma_{na}$  is the capture cross section of electrons by the trap,  $T$  is the temperature,  $E_{na}$  is the energy level of the trap state, and  $k$  is Boltzmann's constant.

Manipulating (13) the energy levels up to the demarcation energy,  $E_e$ , will respond to an AC signal [8]:

$$E_e = kT \ln\left(\frac{\gamma \sigma_{na} T^2}{\omega}\right) \quad (14)$$

where  $\omega$  is  $2\pi f$ .

This demarcation energy level corresponds to a frequency that causes the largest change in capacitance, which also has a thermal dependence. By taking the derivative of the admittance spectroscopy data this frequency can be found [8]:

$$\frac{dC}{dE_e} = -\frac{\omega}{kT} \frac{dC}{d\omega} \quad (15)$$

Using (15) a graph of capacitance peaks can be created. A typical derivative graph for different temperatures is shown in Figure 13.

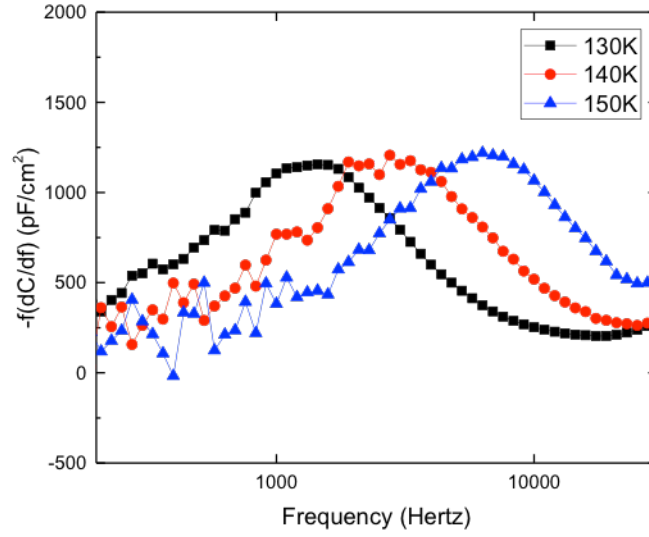


Figure 13. Derivative graph of admittance spectroscopy data used to find the transition frequency.

Once the transition frequency is determined for each temperature, an Arrhenius plot can be made. An Arrhenius evaluates the temperature dependence of the frequency peaks by comparing them to  $1000/T$ . Once the plot is formed, the slope can be used to determine the energy level of the trap. A sketch of an Arrhenius plot is shown in Figure 14.

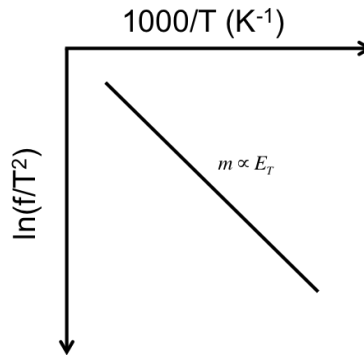


Figure 14. Sketch of an Arrhenius plot, showing that the energy level can be determined by the temperature dependence of trap responses.

## 2.5 Impedance Spectroscopy

Impedance spectroscopy is used to determine the series resistance at a given voltage. Impedance is the measurement of the effective resistance within a circuit. Admittance spectroscopy data can be converted to impedance spectroscopy data by using (10), (11) and the circuit described in section 2.3.3. The derivation is as follows [9].

Impedance is related to admittance by:

$$Y = \frac{1}{Z} \quad (16)$$

where  $Y$  is the admittance and  $Z$  is the impedance.

Using impedance to analyze the model:

$$Z = \left[ \frac{1}{Z_C} + \frac{1}{Z_R} \right]^{-1} \quad (17)$$

where  $Z_C$  is  $\frac{-i}{\omega C}$  and  $Z_R$  is  $R$ .

Simplifying, (17) will become:

$$Z = \frac{R - iR^2\omega C}{1 + (R\omega C)^2} \quad (18)$$

Separating (18) to the real and imaginary values of impedance:

$$Z' = \frac{R}{1 + (R\omega C)^2} \quad (19)$$

$$Z'' = -\frac{R^2\omega C}{1 + (R\omega C)^2} \quad (20)$$

Using (10) and (11), (18) and (19) can be put in terms of admittance:

$$Z' = \frac{1/Y'}{1 + (Y''/Y')^2} \quad (21)$$

$$Z'' = -\frac{Y''/Y'}{1 + (Y''/Y')^2} \quad (22)$$

Equations (21) and (22) describe how the measured values of admittance are converted to impedance. These can then be compared to a circuit model including a series resistor. Standard parallel and series analysis, similar to the analysis above, yields:

$$Z' + iZ'' = R_s + \frac{R_p}{1 + (\omega R_p C)^2} - i \frac{\omega C R_p^2}{1 + (\omega R_p C)^2} \quad (23)$$

Looking at the  $\omega$  dependence of (23), when  $\omega$  approaches zero the real impedance will approach the sum of the series and parallel resistance and the imaginary impedance will approach zero. Similarly, when  $\omega$  approaches infinity the real

impedance will approach the series resistance and the imaginary impedance will approach zero. Using these limits of (23), a form of the equation for a circle is seen:

$$Z''^2 + [(Z' - R_s) - \frac{R_p}{2}]^2 = \frac{R_p^2}{4} \quad (24)$$

The theoretical plot of (24) is shown in Figure 15.

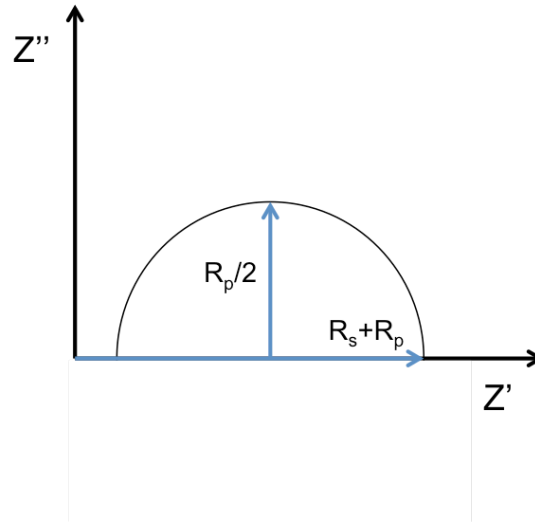


Figure 15. Theoretical impedance curve showing the value of the radius and low frequency limit of  $Z'$ .

From Figure 15 the series resistance can be calculated by determining the radius of the circle ( $\frac{R_p}{2}$ ), determining the diameter ( $R_p$ ) from the radius, then subtracting that value from the low frequency limit of the real impedance ( $R_s + R_p$ ). This value is more simply the x-intercept.

### 3. Experimental Methods

#### 3.1 Preparation for Data Collection

The sample used in this experiment was provided by Bill Shafarman from the Institute for Energy Conversion at The University of Delaware.  $\text{CuIn}_{1-x}\text{Ga}_x\text{Se}_2$  (CIGS) was grown on molybdenum, which were then deposited onto glass substrates. Once the samples were received they were prepped for data collection.

This process starts by scratching a small rectangular perimeter on the sample's surface in order to limit the maximum value of capacitance to be below the systems' maximum measurement values. Another section of the samples' surface was also scratched in order to reveal the molybdenum back contact. The sample was then placed on the end of the probe in Figure 16. When attaching the sample to the probe double-sided Scotch tape was used to ensure the samples' stability. The connection tip was screwed down onto one of the aluminum grid. A copper wire was then soldered to the molybdenum back contact in order to close the sample into the measurement circuit. The sample rod was then placed into the cryostat.

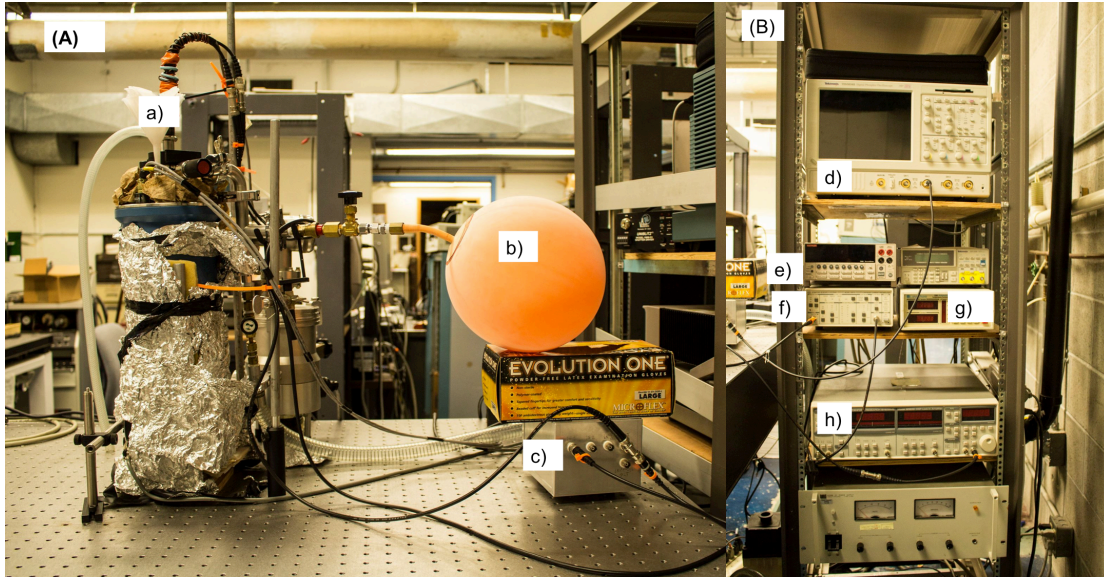


*Figure 16.* Image of the sample attached to the probe, showing the etched square being measured.

The method for preparing the cryostat for cooling samples can be found in the appendix.

Once the cryostat was prepared the sample chamber was flushed with helium gas. This process involves filling the chamber and then pumping the chamber with a vacuum pump for five minutes. Then, helium is used to refill the chamber once again. This process was repeated approximately five times to ensure that the sample

chamber would be filled with only helium. Helium is used for its great performance as a thermal conductor. The cryostat can be used to cool the temperature of the sample from 90K-150K in order to take various measurements of the device. The use of liquid nitrogen allows for this low temperature range. The experimental setup of the cryostat system connected to electronic devices used for data collection is shown in Figure 17.



*Figure 17.* (A) a) Cryostat system with attached b) helium balloon, connected to electronic devices c) adder box, (B) d) oscilloscope, e) DC power supply, f) pre-amplifier, g) temperature control, and h) lock-in amplifier for capacitance data collection.

To further prepare the system, liquid nitrogen was poured into the funnel atop the cryostat. Liquid nitrogen is poured until small droplets escape the exit tube, meaning the coolant chamber of the cryostat is full.

A temperature probe inside the sample chamber was used to monitor the samples' temperature. This probe also allowed for temperature control of the liquid nitrogen. A LakeShore 330 Autotuning Temperature Controller was used to control the temperature of the sample chamber. Since the temperature probe was not located on the sample itself, the system was left to reach equilibrium for approximately thirty minutes to ensure the sample was at the desired temperature.

Once the sample was cooled, measurements could be taken. The measurements used current in order to calculate capacitance at a given time. This was possible due to the lock-in amplifier and pre-amplifier system. A solar cell can be modeled as a capacitor and resistor in series. Capacitance and resistance can be combined to a measurement called admittance. Admittance is the measurement of how easily a circuit allows current flow. The circuit being analyzed is comprised of a resistor in series with a resistor and capacitor in parallel. Within the total admittance the capacitance is  $90^\circ$  out of phase from the resistance values. This comes from how

current flows through a capacitor compared to how the voltage flows through the capacitor. This would attribute resistance to the real value of admittance and capacitance to the imaginary value of admittance. The lock-in amplifier exploits the fact that the total resistance of a circuit and the capacitance of the circuit are out of phase to provide readings of the real and imaginary admittance, whose values are used to calculate the capacitance and conductance of the samples at given frequencies.

### 3.2 Admittance Spectroscopy

Admittance Spectroscopy is used to investigate traps within the bulk material of the solar cell. By adding a DC bias multiple data sets can be collected at once. This would allow for the collection of capacitance as a function of voltage with a constant frequency (Capacitance-Voltage), capacitance as a function of frequency with a constant bias (Capacitance-frequency), and capacitance-frequency data as a function of bias (Capacitance-frequency-Voltage). The data collected was CfV; the rest of the data analyzed was derived from the values measured.

A temperature controller, a DC power supply, a pre-amplifier, and a lock-in amplifier are used for this measurement. The DC power supply ensures that no noise will enter the circuit from the outside. The pre-amplifier and lock-in amplifier allow for the measurement of current, which is then used to calculate the capacitance.

The system was calibrated with a capacitor. The frequency was set to range from 10Hz to 100kHz. Measurements were taken at different temperatures, from 90K to 150K using a 10K step. The process of current measurement and capacitance calculation during the frequency range was done by a computer program. A schematic of the circuit used for admittance spectroscopy is seen in Figure 18.

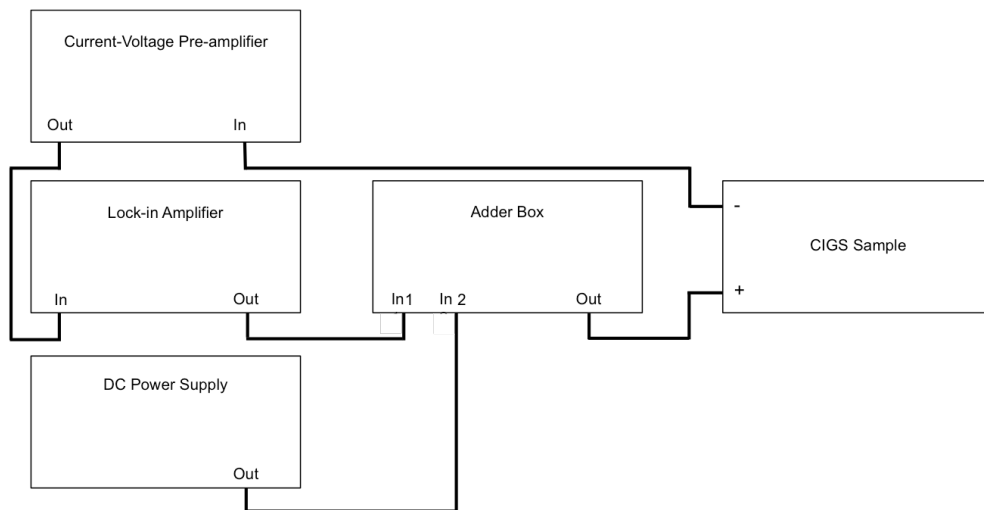


Figure 18. Circuit diagram used for admittance spectroscopy and CfV

## 4. Data Analysis and Results

### 4.1 The Investigation Process

The investigatory process of determining whether the capacitance response in admittance spectroscopy is a response of a back contact barrier or a trap state within the bulk material will be outlined.

The first analysis done was Capacitance-Voltage. This analysis is used in order to investigate the presence of a roll over in the capacitance measurement similar to that of the double-diode model. The collected Capacitance-Voltage data did provide evidence that a back contact barrier could be present. However can the back contact rollover provide the capacitance response in admittance spectroscopy?

In order to answer this question admittance spectroscopy was measured as a function of DC bias, previously referenced as Capacitance-frequency-Voltage. This technique is adding a DC bias dependence to admittance spectroscopy. Admittance Spectroscopy allows for the measurement of the energy of a trap state using the transition frequency of the capacitance step. If a DC bias is applied to the sample and admittance spectroscopy data is taken the energy level of a trap at different parts of the sample can be measured. If the back contact barrier is contributing to the capacitance response in admittance spectroscopy, it is expected that there would be a significant shift in the energy level measured at high forward bias compared to reverse and minor forward bias. The expected shift in energy level was not seen in the data, however negative capacitance was measured at low frequencies, shown in Figure 20. The rollover in Capacitance-Voltage was especially present at low frequencies, shown in Figure 19. Could the presence of negative capacitance cause the roll over in the Capacitance-Voltage data? Better yet, is the presence of negative capacitance a plausible phenomenon?

The answer to this question comes from the experimental testing of the model [7] discussed in Section 2.3. First the admittance spectroscopy data were converted to impedance spectroscopy data. Impedance spectroscopy allows for circular plots to be formed in which the series resistance can be calculated [9]. The derivation of this analysis was discussed in Section 2.5. The model states that if a series resistance is exponentially proportional to the DC current and inversely exponentially dependent on DC voltage (the applied bias), negative capacitance can be measured. Those two dependencies of series resistance are two ways to investigate one parameter, one in the DC regime and one in the AC regime. A series resistance that is inversely exponentially dependent on the applied bias is measured in the AC regime. A series resistance that is exponentially proportional to DC current is measured in the DC regime. Series resistance values were collected and analyzed, giving experimental evidence that negative capacitance is a plausible phenomenon and that the



capacitance response in admittance spectroscopy is not a result of a back contact barrier.

The data and results of the investigation are in the following sections.

## 4.2 Capacitance-Voltage

Capacitance voltage data were extracted from admittance spectroscopy data for multiple frequencies. These data were graphed and are shown in Figure 19.

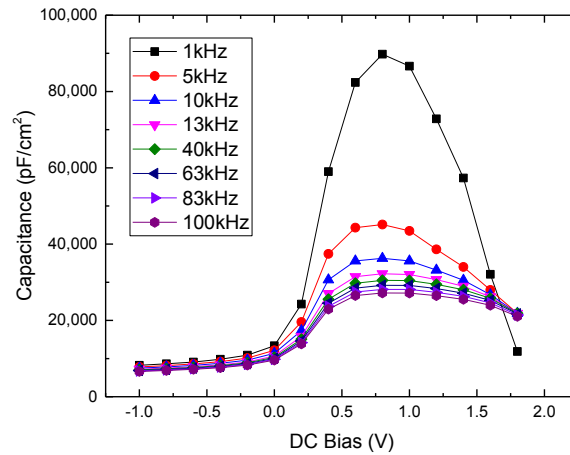


Figure 19. Capacitance voltage data with multiple frequencies displaying the presence of a back contact barrier.

The capacitance voltage response is as expected from the double diode model, where there is a rollover of the capacitance measurement starting around 0.8V for each frequency. However it is more prevalent at low frequency measurements. The relation to the double diode model indicates a presence of a back contact barrier.

## 4.3 Capacitance-frequency-Voltage

### 4.3.1 Capacitance Response as a Step

Admittance spectroscopies with applied DC biases ranging from -1.0V to 1.8V were collected for temperatures between 120K and 150K. The data for 130K are shown below in Figure 20.

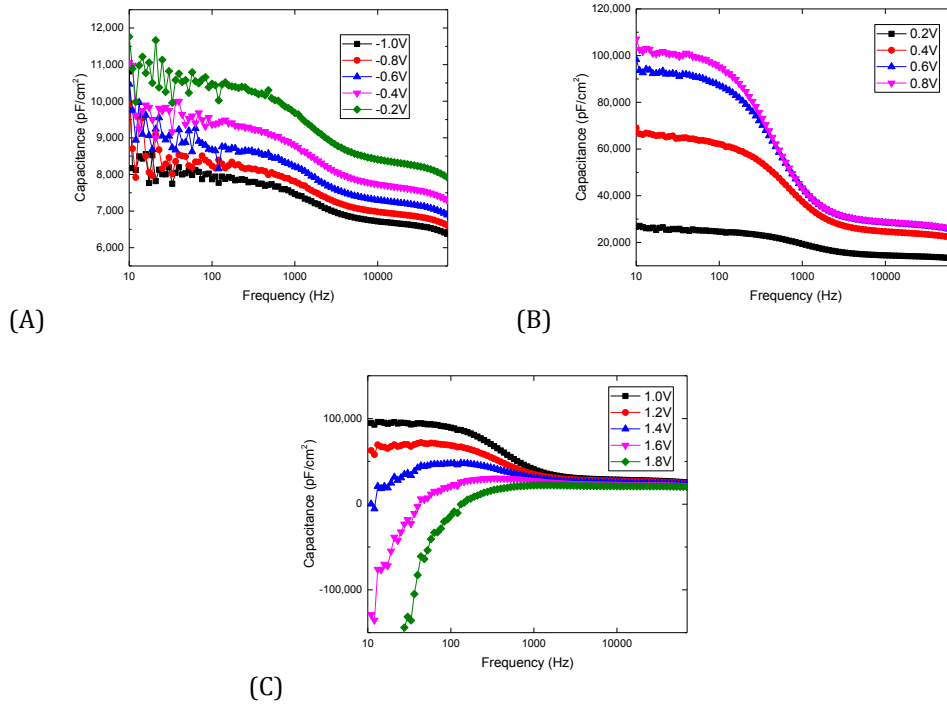


Figure 20. (A) Capacitance frequency graph corresponding to reverse bias, (B) minor forward bias, and (C) high forward bias at 130K.

The capacitance response, shown as a step in admittance spectroscopy data, can be seen in the reverse bias, minor forward bias, and the high forward bias range plots, until the applied forward bias is larger than 1.0V. The shift of the capacitance step out of the observable frequency range is expected, however further analysis of the energy level at each bias is required in order to make conclusions. The next step in the analysis is to take the derivative of each admittance spectroscopy in order to see the capacitance response as a peak.

#### 4.3.2 Capacitance Response as a Peak

The derivative of capacitance with respect to frequency was taken. The data was smoothed using a moving average. If there is a large shift in the transition frequency moving from reverse bias to high forward bias, then the back contact barrier could be seen taking over the capacitance measurements. The graphs showing the transition frequency as a peak with corresponding bias ranges are in Figures 21-23.

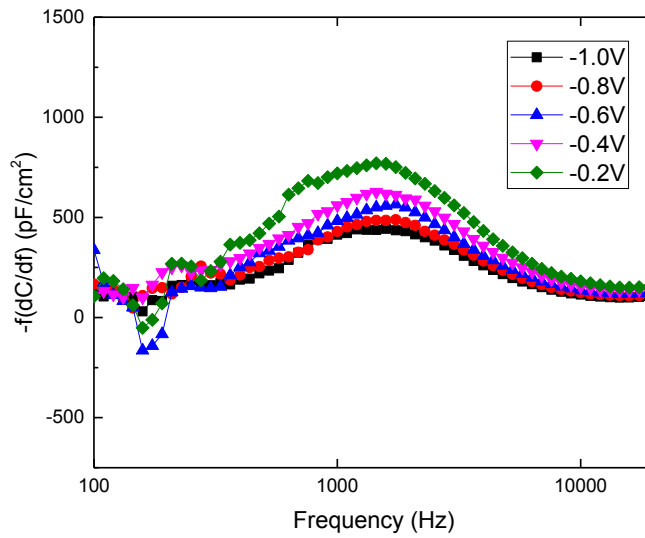


Figure 21. Derivative analysis graph for reverse biases at 130K, used to determine the transition frequency.

For the reverse bias range the transition frequency remains around 1kHz, meeting the expectations of a constant trap state energy level.

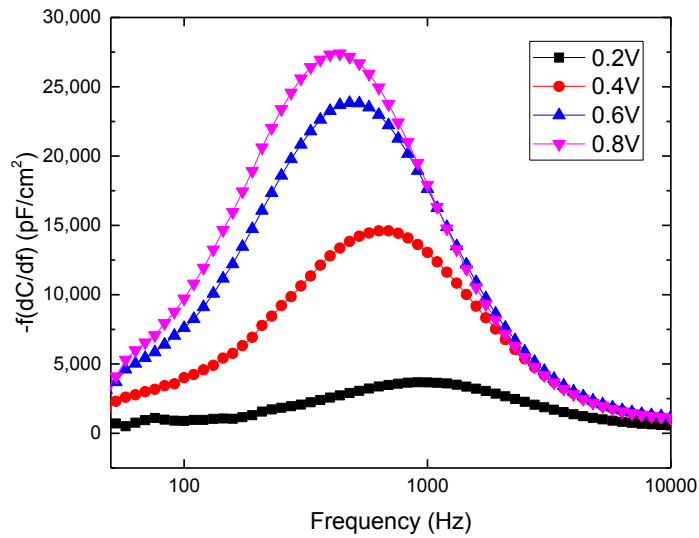


Figure 22. Derivative analysis graph for minor forward biases at 130K, used to determine the transition frequency.

For the minor forward bias range the transition frequency has a slight shift but stays relatively constant at 1kHz. The slight shift is insignificant in the broad analysis of the energy level. If the back contact barrier was being observed in this range of bias,

it is expected that the shift in transition frequency would be much larger than seen in Figure 22.

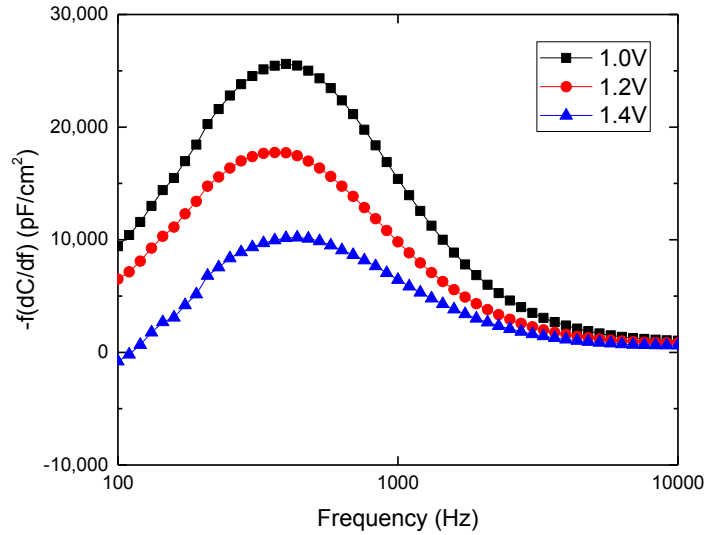


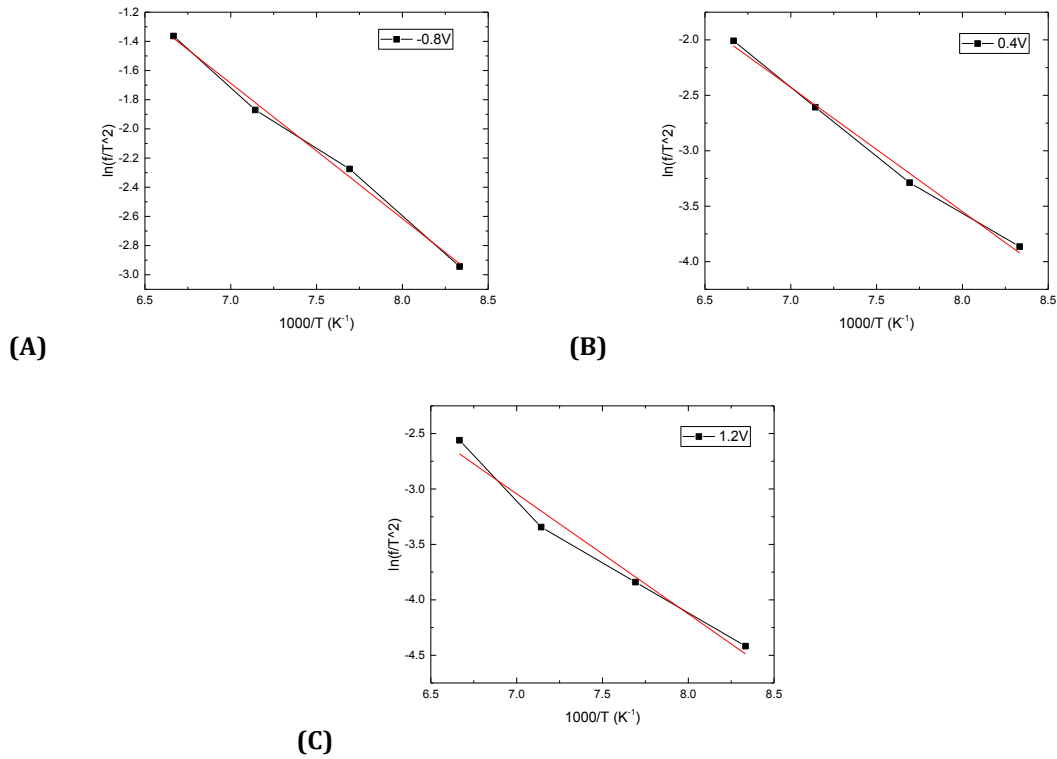
Figure 23. Derivative analysis graph for high forward biases at 130K, used to determine the transition frequency.

For the high forward bias range the transition frequency shifts off of the graph, suggesting the presence of a back contact barrier. However negative capacitance presents itself at forward biases above the built in potential,  $\approx 0.8V$ . This effect could have an impact of the rollover seen in the Capacitance-Voltage data, giving a false response of a back contact barrier. Further analysis of the presence of negative capacitance is in the following section.

Continuing the analysis of energy levels at each applied bias, the peak frequencies will be plotted versus temperature. The slope of these plots will be used to determine the energy level.

#### 4.3.3 Determining the Energy Level

The peaks in Figures 21-23 correspond to transition frequencies at each applied bias. Using the transition frequency determined for each temperature, an energy level corresponding to an applied DC bias can be determined. The energy level is determined from the slope of an Arrhenius plot. An Arrhenius plot is plotting some variable versus  $1000/T$ , in order to analyze the temperature dependence. Example Arrhenius plots for bias ranges are shown in Figures 24.



*Figure 24.* Arrhenius plots for (A) reverse bias of -0.8V. The slope of the trend line corresponds to an energy level of 79.88 +/- 3.84 meV (B) minor forward bias of 0.4V. The slope of the trend line corresponds to an energy level of 96.5 +/- 5.6 meV (C) high forward bias of 1.2V. The slope of the trend line corresponds to an energy level of 93.3 +/- 10.2 meV.

Arrhenius plots for each applied bias were created. From each plot the energy level of the supposed trap state were calculated. The energy levels were graphed versus the applied DC bias to see if there was a significant shift in energy levels when the sample was put into high forward bias, indicating a back contact barrier. This plot is seen in Figure 25.

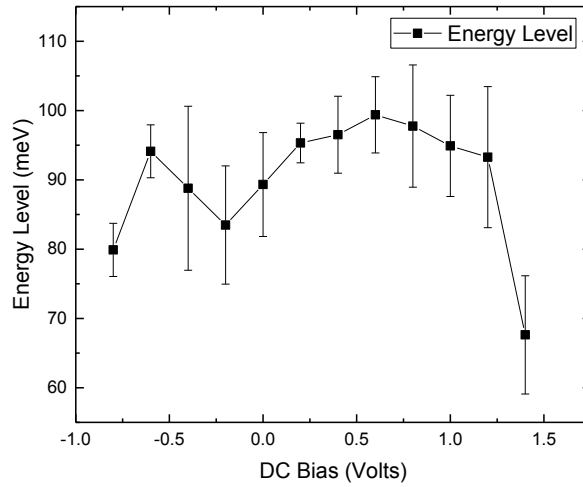


Figure 25. Energy level of observed trap state versus applied DC voltage including standard error.

The energy level in reverse bias stays relatively constant as expected. The energy level has a slight increase in the minor forward bias range; this can be explained by a slight change in the localized trap state within this part of the material. The energy level then decreases at high forward biases and returns to a level that is consistent with the reverse bias energy levels. If a back contact barrier were present the energy level at high forward biases would be significantly different from that of reverse biases.

It cannot be said if the back contact barrier is or is not being measured. This uncertainty comes from the presence of negative capacitance. The negative capacitance phenomenon seems to be dominating the capacitance measurements, leading to a misleading response of a back contact barrier within the capacitance voltage data.

The model that allows negative capacitance [7] needs to be experimentally tested using impedance spectroscopy. If the data shows a series resistance that is heavily dependent on voltage, then previously believed back contact barrier response in the capacitance voltage data cannot be contributed only to the back contact barrier. This would mean that the AC measurements of capacitance only allow for the analysis of a trap state within the bulk material of the sample.

## 4.4 Impedance Spectroscopy

Impedance spectroscopy data were extracted from admittance spectroscopy data. The data were then plotted, demonstrating circular plots as expected. Circular plots for each bias range are shown in Figure 26.

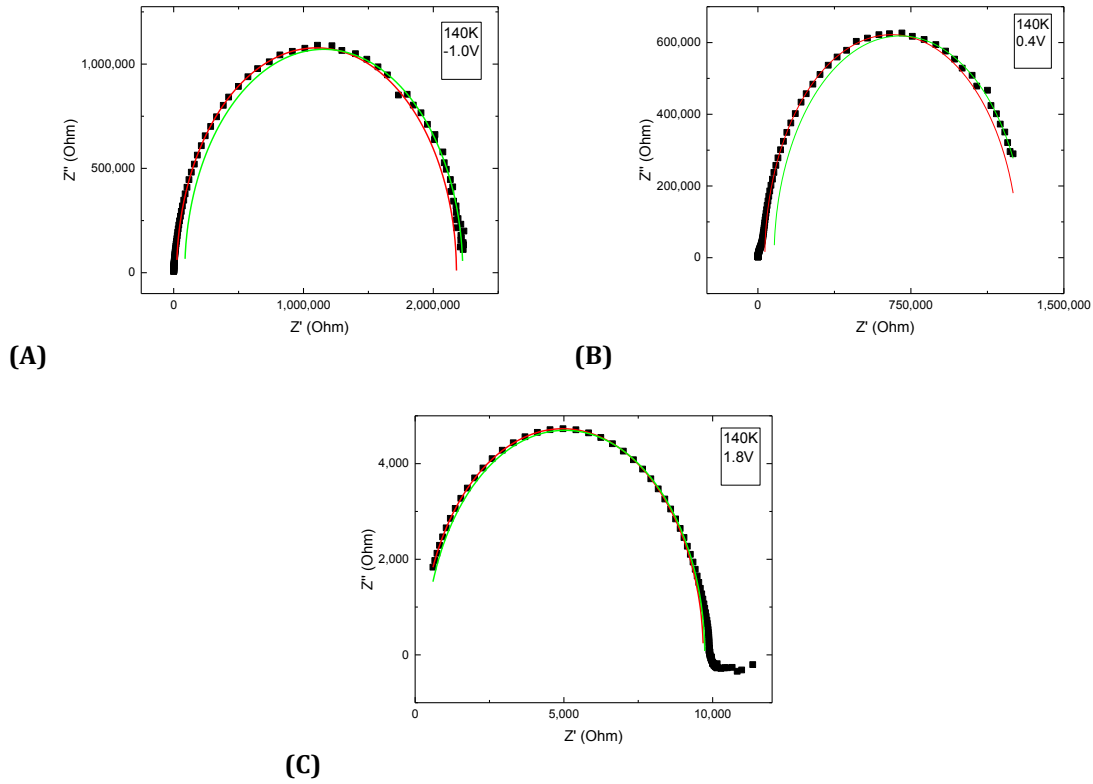


Figure 26. Impedance curve for (A) reverse bias of -1.0V (B) minor forward bias of 0.4V (C) high forward bias of 1.8V at 140K with circular fits to high and low frequency ranges.

The circular fits correspond to high (red) and low (green) frequencies, showing two different circles. In order to create the circular fits the frequency range had to be separated into high and low frequencies. Once split, the data were compared to that of a circle. The theoretical fits then correspond to the equation of a circle that best fit the data for the given frequency range. This means two different series resistance values are measured. Negative capacitance is seen as a low frequency response; therefore the low frequency circular fit series resistance values are used in the analysis.

Series resistance values were determined for each applied DC bias, for each temperature. The series resistance measured was graphed versus the applied DC bias, as seen in Figure 27.

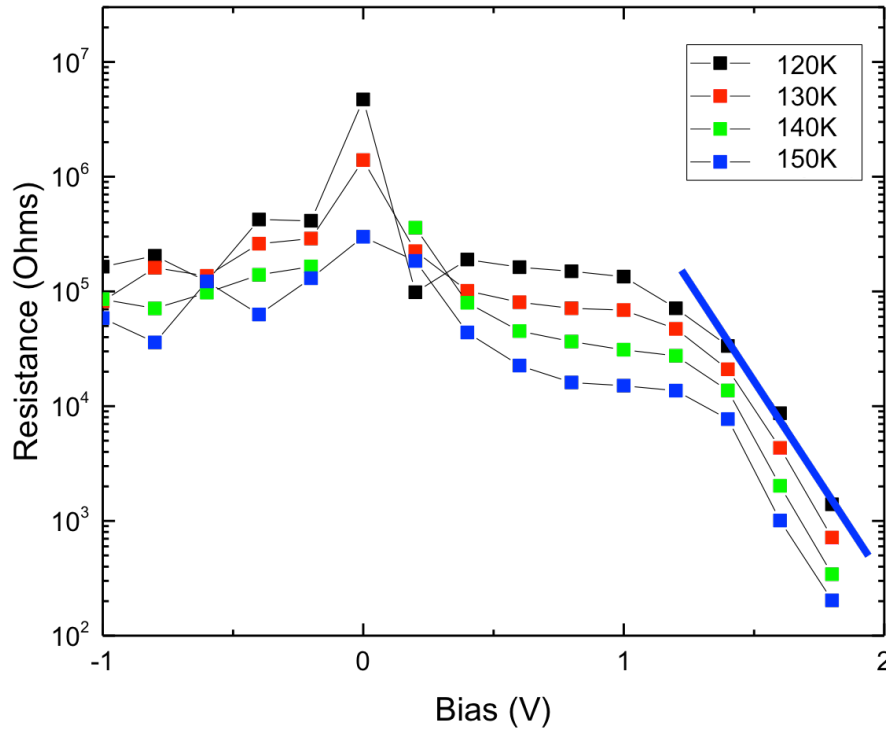


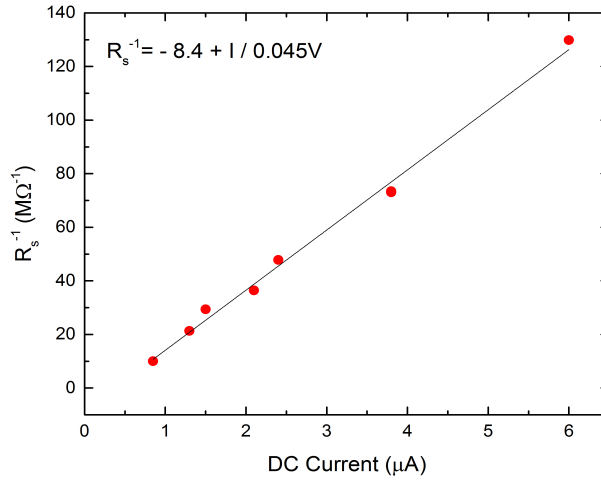
Figure 27. Plot of series resistance versus applied DC bias, demonstrating an exponential decrease in series resistance with an increase in applied DC bias in the high forward bias range.

There are two ways to measure the one parameter that needs to be met in order to have experimental evidence for the negative capacitance model, one AC and one DC. The AC explanation is a series resistance that is inversely exponentially dependent of applied DC bias. The DC explanation is a series resistance that is exponentially proportional to the DC current. More specifically the proportionality between series resistance and DC current must be larger than  $kT$ .

Looking at the high forward bias range in Figure 27, there is an apparent linear decrease in series resistance with respect to applied DC bias. However, since this graph is on a semi-log plot, meaning that the linear decrease in series resistance is actually an exponential decrease. This data experimentally meets the AC explanation of the negative capacitance model.

Alex Ogle [10] collected and analyzed current voltage data. Using the DC current data along with the measured AC series resistance, from impedance spectroscopy, the second parameter can be analyzed. The plot of DC current with AC series resistance is seen in Figure 28.





*Figure 28.* DC current versus inverse of AC series resistance at 120K to determine whether the proportionality is congruent with the second parameter of the model.

The slope of Figure 28 is the proportionality factor between DC current and AC series resistance. The value of the proportionality factor is 0.045eV. The data in Figure 28 were taken at 120K. The value of  $kT$  at 120K is approximately 0.01eV. The proportionality factor is larger than  $kT$ , meaning that the data experimentally meets the second parameter of the model. Conclusions about whether the AC measurements of capacitance allow for the detection of a back contact barrier can now be made.

## 5. Conclusion

The results presented in this paper tell us that a back contact barrier response cannot be investigated using Capacitance-Voltage analysis alone. In our sample, the rollover in Capacitance-Voltage that was previously explained as a back contact barrier response is actually an effect of negative capacitance from a series resistance that is heavily dependent on voltage.

Further use of the series resistance values determined in this paper would be to correct data in order to further investigate the main diode of the sample. Negative capacitance was seen in a previous sample, however there is not enough Capacitance-frequency-Voltage data to analyze the phenomenon. Further analysis of the previous sample and other samples at high forward bias could be performed in order to add to the discussion of minority carrier transport and even charge carrier dynamics in general.

## 6. Appendix

### 6.1 Outgassing the Diffusion Pumps

In order to prepare the cryostat system for cooling, one should carefully follow the steps listed below (approximately once per week):

1. Make sure there is no liquid nitrogen within the system. If there is liquid nitrogen in the system, it must be allowed to sit over night and evaporate.
2. Make sure the Turbo Pump is connected properly.
3. Check that the Thermos Valve is closed.
4. Close the Vent and Gate Valves.
5. Check that the water level of the Turbo Pump fills 2/3 of the tank.
6. Turn on the Roughing Pump for 5-10 minutes.
7. Open the Gate Valve, then open the Thermos Valve. Wait 10 minutes.
8. Push start on the Turbo Pump. The “normal” light should become illuminated. If the “failure” light illuminates, turn off the Turbo Pump.
9. Check the power supply connected to the collection sponge. This is the big power supply on the bottom of the electrical equipment shelf.
10. Start the power supply at 5V and wait approximately 30 minutes. Once the time has elapsed, up the voltage to 10V and wait 30 minutes. Once 30 minutes has elapsed, up the voltage to 15V and wait a very long time.
11. Close the Thermos Valve. Once the Thermos Valve is closed, the Turbo Pump will begin to gurgle. When the gurgling happens, close the Gate Valve and immediately shut down the Turbo Pump.
12. The cryostat system is now ready to be filled with liquid nitrogen and begin to cool samples.

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